ABSTRACT

Title of Thesis:	EXPERIMENTAL QUALIFICATION ASSESSMENT AND FAILURE ANALYSIS FOR REWORKED AND TRIMMED EMBEDDED RESISTOR TECHNOLOGIES
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Discrete passive components are continuing to increase in use in electronic systems even though manufacturers are increasing the degree to which these systems are integrating. Driven by performance, size and economic concerns, embedded passives were introduced to the market in the early 1980s. However, significant obstacles to characterize, evaluate and integrate embedded passives must be overcome before widespread adoption is realized.

This thesis explores the reliability concerns and subsequent failure assessment for variously configured, reworked and trimmed Gould subtractive nickel chromium and MacDermid additive nickel phosphorous embedded resistor technologies within a printed wiring board substrate. Environmental qualification included: thermal characterization,

stabilization baking, temperature cycling, thermal shocking and temperature/humidity aging. In addition, a pre/post lamination analysis is included along with a systematic three level hierarchical failure analysis to extract critical failure mechanisms induced through environmental qualification. Ultimately, a material stability assessment and comparison with well established discrete resistor technologies was achieved.

EXPERIMENTAL QUALIFICATION ASSESSMENT AND FAILURE ANALYSIS FOR REWORKED AND TRIMMED EMBEDDED RESISTOR TECHNOLOGIES

by

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"I have been crucified with Christ; it is no longer I who live, but Christ lives in me; and the *life* which I now live in the flesh I live by faith in the Son of God, who loved me and gave Himself for me."

-- Galatians 2:20

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1 INTRODUCTION

1.1 PASSIVE COMPONENTS

By definition, passive components are devices that dissipate power or store energy, as opposed to active devices, such as transistors, that generate power gain [Whitaker 1996]. Traditional passives are discrete devices that are either through-hole or surface mounted onto a substrate. The most common examples of passive components are resistors and capacitors; however, inductors and diodes are also considered passive devices. Passive components are manufactured in many physical forms including discretes, arrays and networks, integrated passive devices and embedded passives. Table 1.1 compares each physical form for several selection criteria.

Passive devices are often referred to as "glue components" since they, in essence, "glue" integrated circuits (ICs) together to generate electronic systems. In order to transfer electronic signals between ICs without excessive signal degradation, passive components perform many vital functions including:

Decoupling (Bypassing) – Switching noise originates when drivers switch current through inductances that are present in board interconnections, power and ground deliveries to the board, die to package bonds or parasitics in single chip packages. Switching noise causes variations in the potential difference between power and ground planes and can result in false switching of logic circuits and signal delays. Switching noise is controlled by adding capacitance that supplies electrical charge that compensates

Table 1.1: Passive component's physical forms caparison [Marcanti *et al.* 2001]

	Discretes	Arrays and Networks	Integrated Passive Devices (IPD)	Embedded (Integral) Passives
Definition	A single passive element (capacitor, resistor or inductor) in a leaded or surface mount case.	Passive arrays combine multiple passive elements of like function (e.g., all capacitors or all resistors) in a single surface-mount case. Networks combine passives of more than one function (e.g., capacitors + resistors) in a single surface-mount case. A network typically contains 4 to 12 elements.	Multiple passive elements of more than one function and possibly a few active elements (e.g., capacitors + resistors + transistors) in a single surface-mount or CSP. Typically an IPD contains more than 20 elements. IPDs may also be referred to as "super components."	Passive devices that are buried in the substrate material rather than being surface mounted on top.
Cost	Good – The benchmark for all other technologies.	Better – When local densities have 4 to 8 devices close together.	Better – When high local densities are application specific.	Better – When average component density is above 3 devices/cm^2. Cost is panel size dependent.
Size	Good – Board area required for each and every device.	Better – 50% and greater board area savings over discretes.	Better – Application specific IPDs can replace dozens of components.	Best – No surface board area required because the devices are buried.
Performance	Good – Self-resonates at low frequencies.	Good – Self-resonates at low frequencies.	Better – Qualified out to several gigahertz (GHz)	Best – Ideal components; when buried underneath the IC, it serves mainly to decrease lead length and avoid build up inductance of the connection loops.

	Discretes	Arrays and Networks	Integrated Passive Devices (IPD)	Embedded (Integral) Passives
Reliability	Good – Heavy use of solder joints.	Better – Reduces solder joints slightly.	Better – Significantly reduces solder joints.	Best – Elimination of solder joints.
Flexibility	Best – Flexible for both design and manufacturing.	Better – Than IPDs and embedded passives.	Better – Than embedded passives.	Good – Requires modeling and simulation.
Time to Market	Best – Flexibility allows quick turns.	Better – Simple quad and octal arrays can be designed in quickly.	Good – IPDs require additional design iterations for wireability.	Fair – Most board shops require at least 5 to 7 days to fabricate an embedded passives board.
Availability	Best – Highly available from multiple sources.	Better – Standard parts from multiple suppliers.	Better – Non-standard parts from multiple suppliers.	Fair – Few suppliers.
Values	Best – All values available at commodity prices.	Better – Thick film arrays offer high values.	Good – Thin films have limited capacitor values.	Good – Currently limited to low values.
Tolerances	Best – Tight tolerances at commodity prices.	Better – Both offer tight tolerances.	Better – Thin films offer tight tolerances.	Good – Loose tolerance, generally 5 to 10%.

for perturbations in the power/ground delivery system. The capacitance is supplied using a combination of coupled power and ground planes and discrete capacitors connected between power and ground.

Line Termination – Impedance mismatches in transmission systems cause a portion of the signal propagated on the line to be reflected back to its source. Reflections cause noise that contributes to false switching and delays, and becomes an increasingly critical performance driver as frequency increases. Transmission lines are terminated with resistance to match impedance thereby minimizing the reflected signal. Lines can be series terminated by placing resistance within the line or parallel terminated by placing resistance at the end of the line. The resistance can be supplied by either discrete resistors or by losses in the transmission line itself, e.g., self-termination.

Pull-up – Pull-up resistors are extremely common in digital circuits. The key function for a pull-up is to prevent input lines from floating, thus insuring that given no other input, a circuit assumes a default value. The key function for the pull-up resistor itself is to prevent too much current from flowing through the pull-up circuit. Actually, there are two types of circuits, pull-up and pull-downs. Their function is the same, to create a default value for a circuit, but one pulls the line high, while the other pulls it low.

Electrical filters – Because power supplies and the power distribution system on a board are not ideal, each circuit or group of circuits is decoupled to minimize noise coupling through the supply system. Resistor-capacitor and inductor-capacitor decoupling

networks can be used to isolate circuits from the power supply, eliminate coupling between circuits and keep power supply noise from entering the circuit.

1.2 PASSIVE GROWTH

Discrete passive components are continuing to increase in use in electronic systems even though manufacturers are increasing the degree to which these systems are integrating. Higher performance systems and smaller form factors are driving towards passive integration; however, according to a recent study by *Prismark Partners, LLC.*, in 2001 alone, approximately 1 trillion passive components were consumed with only 26 billion, or 2.6%, passive devices integrated in some fashion [Prismark 2001]. While many analysts believed discrete passives would "integrate" away into integrated circuits, exactly the opposite has occurred [Sandborn *et al.*2001]. In 1984, passive devices represented 25% of all components on printed wiring boards; by 1998 this fraction grew to over 90% (Figure 1.1). In 2001, passive devices accounted from 91% of all the components, 41% of the board area and 29% of all solder joints in an electronic system [Prismark 2001].

Although passive integration has increased dramatically in products, especially in hand-held devices and computers since 1996, the number of passive components is still greater than 80% of the total part count and the passive-to-active ratio continues to escalate as well [Tummala *et al.* 2000]. According to the 1998 National Electronics Manufacturing Initiative (NEMI) roadmap for passive component technologies, an estimated 55 billion surface-mount discrete passive resistors and capacitors were replaced

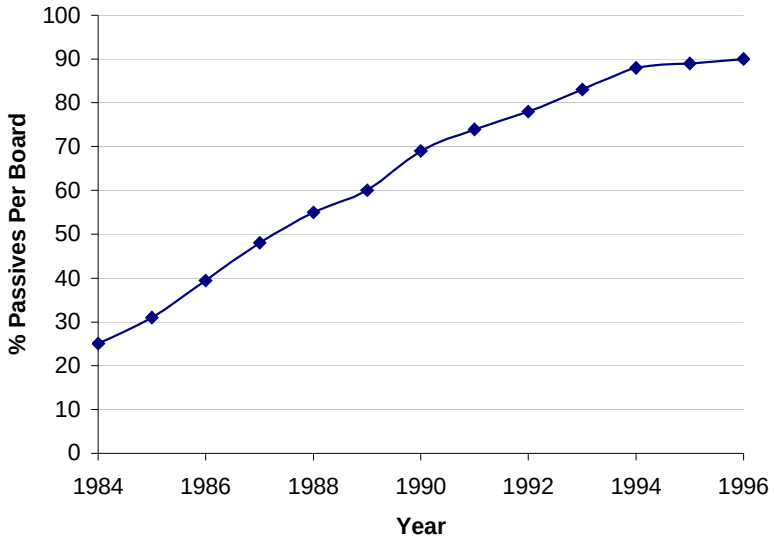


Figure 1.1: Growth of passive components in electronic systems [Lasky 1998]

with higher levels of integration in 1998 [NEMI 1998]. Meanwhile, Table 1.2 illustrates the imbalance still witnessed by these industries driven by consumer demand for faster clock speeds, lower operating voltages, higher I/O counts and combined analog and digital functionality.

According to strategic research by *Frost & Sullivan*, total revenues for discrete resistors reached $5.1 billion in 1997, revenues accumulating $1.4 billion in North America alone [Frost & Sullivan 1998]. The resistor market in North America is expected to continue to be driven by the telecommunications can computer industries, while in Europe high labor costs and a soft market for resistors will restrain market share, according to *Frost & Sullivan* analysts Keith Robinson. Southeast Asia holds the largest share of the market at 47.1%, and it is driven by strong demand in the consumer

Table 1.2: Passive-to-active ratio of recent products [Rector 1998]

System	Total Passives	Total ICs	Ratio
Cellular Phones			
Ericsson DH338 Digital	359	25	14:1
Ericsson E237 Analog	243	14	17:1
Philips PR93 Analog	283	11	25:1
Nokia 2110 Digital	432	21	20:1
Motorola Mrl 1.8 GHz	389	27	14:1
Casio PH 250	373	29	13:1
Motorola StarTAC	993	45	22:1
Matsushita NTT DoCoMo	492	30	16:1
Consumer Portable			
Motorola Tango Pager	437	15	29:1
Casio QV10 Digital Camera	489	17	29:1
1990 Sony Camcorder	1226	14	33:1
Sony Handy Cam DCR-PC7	1329	43	31:1
Other Communication			
Motorola Pen Pager	142	3	47:1
Infotac Radio Modem	585	24	24:1
Data Race Fax-Modem	101	74	7:1
PDA			
Sony Magic Link	538	74	7:1

electronics industry [Frost & Sullivan 1998]. Table 1.3 provides a market forecast for passive arrays into 2004.

Why is the increased demand for passive devices not met by fabricating passives within ICs? Oddly, the answer lies within the fact that some passive devices are, in fact, fabricated within ICs; however, designing passives into ICs limits the IC's flexibility for multiple uses, e.g., typically one IC is designed for many intended purposes while the specific application determines the necessary "passive tuning." In addition, real estate on an IC is often more expensive than real estate on a board.

The trend shown in Figure 1.1 not only requires more passives to be purchased and assembled to the system, but it also requires increased board area, demonstrated by a

Table 1.3: Passive Array Forecast [Prismark 2001]

	2000		2004	
	Units*	**Value****	**Units***	**Value****
Resistor Chip Arrays	6.60	$99.0	10.8	$140.0
Capacitor Chip Arrays	1.47	$102.6	2.36	$145.0
R/C Networks and Arrays (Chips)	0.36	$33.0	0.58	$46.6
Total Chip Arrays (Chips)	8.43	$234.6	13.74	$331.6
Total Thin Film Arrays and Networks	0.85	$55.0	2.0	$105.0
Total Arrays (Thick and Thin Film)	9.28	$289.6	15.74	$436.6

* Billion

** Million

Prismark Partners, LLC., case study on the cellular phone industry, the most complex, high volume electronic system to date [Prismark 2000]. In 1995, less than 5 passives per square centimeter was dedicated area whereas reasonable estimates into 2010 project a passive component density of approximately 22 passives per square centimeter (Figure 1.2).

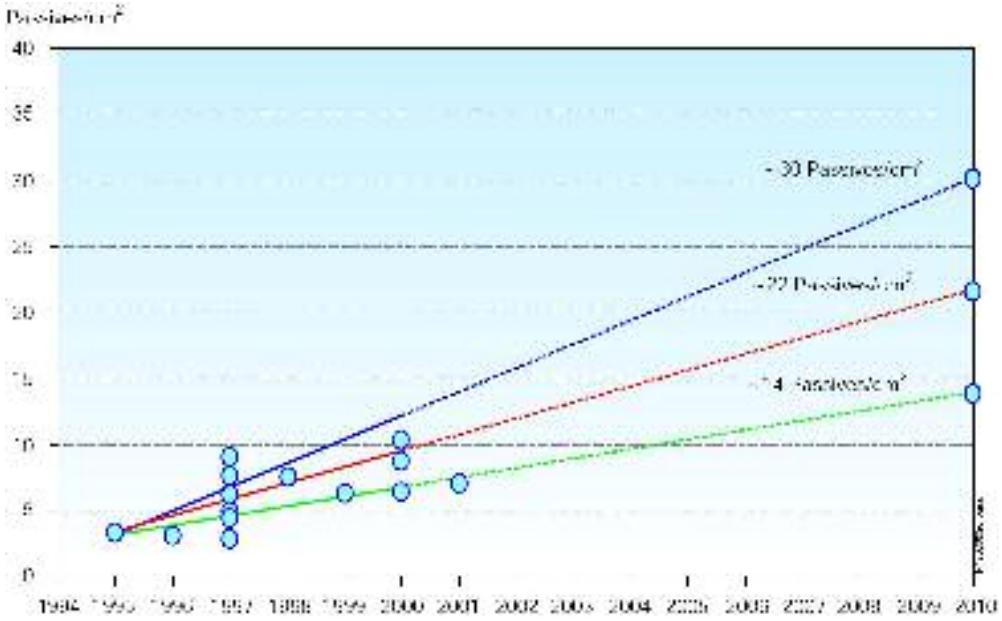


Figure 1.2: Cellular phone passive density over time [Prismark 2000]

The electronics assembly industry's response to the challenges of passive growth in systems was the development of higher-speed chip sorters with placement speeds greater than 100,000 placements per hour. The passive components industry has also responded by producing smaller passive components. Figure 1.3 documents market share for various size passive components.

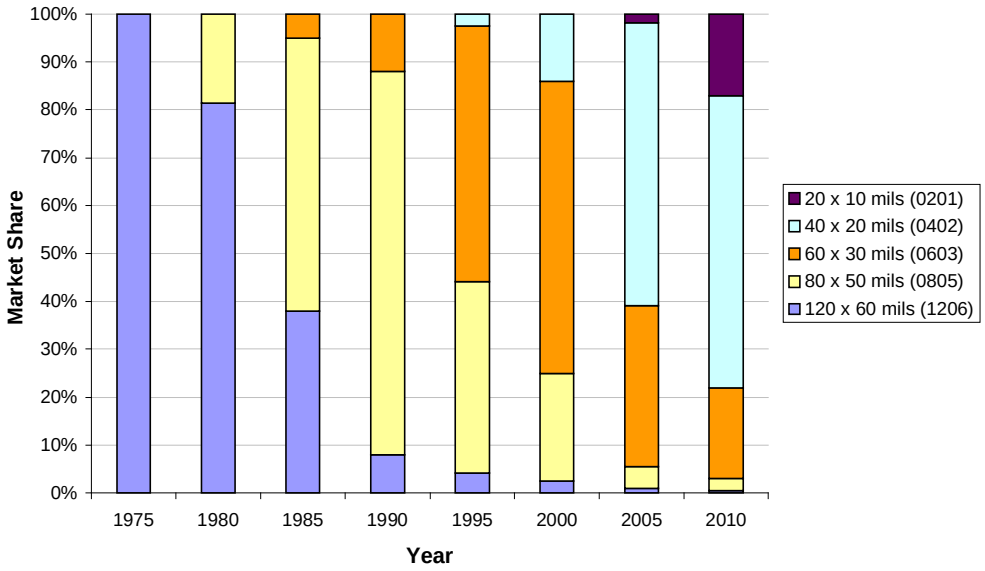


Figure 1.3: Trends in passive device size [Lasky 1998]

Another solution to accommodate passive growth is integrating multiple passives together within a single package assembled as networks or arrays of passives. This approach can reduce assembly costs; however, the per unit cost of integrated passives remains high, even higher than the discrete passive components they replace. Even with the use of small dimension passives and judicious insertion of network array passive components, many applications still cannot meet performance and size design constraints. Embedded passives (EPs) were introduced to address these requirements. Embedded

passives are fabricated within substrates, and while EPs will never replace all passive components, they provide a potential advantage for many applications.

1.3 EMBEDDED PASSIVES

1.3.1 Overview

The only logical future direction for passive components is to go inside the interconnecting substrates of the printed wiring board [Passive 2000]. Embedded passives, also known as integral passives, are passive components buried in interconnecting substrate materials, e.g., FR4. The defining characteristic for embedded passives is the fact that the device does not need to be mounted on or connected to the exposed substrate surface [Marcanti *et al.*2001]. Manufacturers' expectations for embedded passives is to form the components from substrate materials or fabricate low-profile, flexible components placed within the printed wiring boards during the manufacturing process. A white paper produced by DuPont *i*Technologies describes a strategy and approach for creating embedded passive material standards and guidelines for design [McGregor 2001]. Market potentials for embedded passive components are estimated to exceed $2 billion within the next 10 years. Although capacitors, resistors and inductors are all candidates from embedding, current interests are focusing on capacitors and resistors since they represent the majority of passive devices used on a circuit board. Both buried resistors and capacitors can be fabricated in singulated value form while capacitors can also be manufactured in distributed planar form. Figure 1.4

illustrates a printed wiring board containing embedded passive components freeing up valuable substrate real estate which in turn is consumed by more important surface mount chips. Thin-film passive components rely on deposition and photolithography to physically define conductive, resistive and dielectric materials that produce a desired electrical response [Lenihan *et al.* 1996]. Even though the actual film technology is dated, current research focuses on optimizing the materials according to application specific requirements.

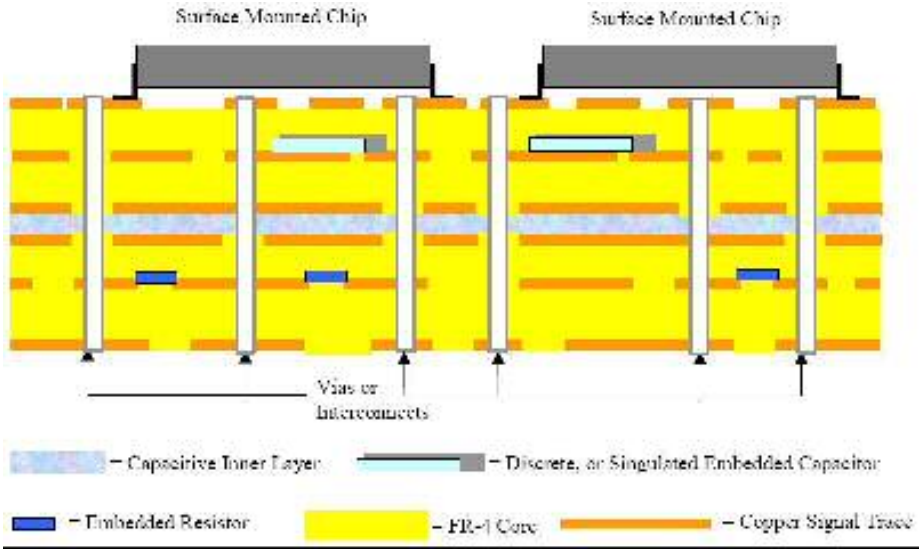


Figure 1.4: Cross-sectional view of a printed wiring board [McGregor 2001]

1.3.2 Embedded Resistors

Embedded resistors are manufactured from both thick and thin-film technologies by depositing and pattering square layers of resistive material in conjunction with an interconnecting line within a substrate (Figure 1.6, Trim Figure A). For thin film applications, the thickness varies from a few tens of nanometers to several microns while

thick films range from 10 to 50 microns [Ulrich *et al.*2000]. The primary driver for replacing surface-mount resistors with embedded resistors is faster bus speeds. As bus speeds exceed 10 MHz, the number of resistors to manage the electronic system becomes rather large. In order to quell transmission times and improve performance, embedded resistors can be buried in the substrate to eliminate extraneous distances generated by interconnects. In addition, embedded resistors free valuable board area and possibly improve reliability through the elimination of solder joints and plated through-holes characteristic of surface-mount and through-hole technologies. The resistance (R) of particular material is given by Equation 1:

$$R = \frac{\rho L}{Wt}, \qquad \textbf{(Equation 1)}$$

where,

R = resistor value (Ω)
ρ = bulk resistivity (Ω∗m)
L = resistor length (m)
W = resistor width (m), and
t = resistor thickness (m)

However provided the resistor thickness is constant, Equation 1 reduces to,

$$R = \frac{\rho_s L}{W} = \rho_s N, \qquad \textbf{(Equation 2)}$$

where,

ρ_s = bulk resistivity (Ω∗m), and
N = aspect ratio defining number of square resistive elements
= $\frac{L}{W}$

Thus, in order to obtain a desired 50 O resistor, 1 square (determined by the aspect ratio of the patterned resistor) of a 50 O/square sheet resistive material is needed. By linking squares together, using square portions or even creating different aspect ratios, it is possible to achieve different resistor values. Figure 1.5 illustrates three different resistor arrangements available.

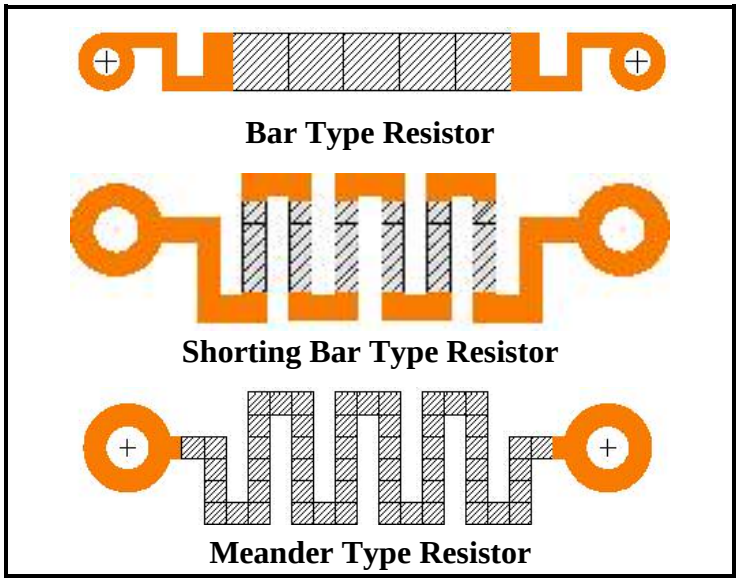


Figure 1.5: Embedded resistor designs [Ohmega]

Furthermore, high precision laser trimming of buried resistors can tailor resistance values within less than 1% tolerance of target values [Fjeldsted *et al.*2002]. Figure 1.6, depicts several trim shapes available for selection depending on specific design requirements.

Various materials used to manufacturer embedded resistors can be found in Appendix A, Table A.1. Two approaches to develop embedded resistors are additive and subtractive. Additive methods deposit resistive materials to existing innerlayer pairs

using plating or printing techniques. Meanwhile, subtractive methods dedicate a layer pair in which material is removed from the substrate to form individual embedded resistors using etching techniques. Table 1.4 highlights companies involved in embedded resistor technologies, the materials they manufacture and their corresponding approach for fabrication.

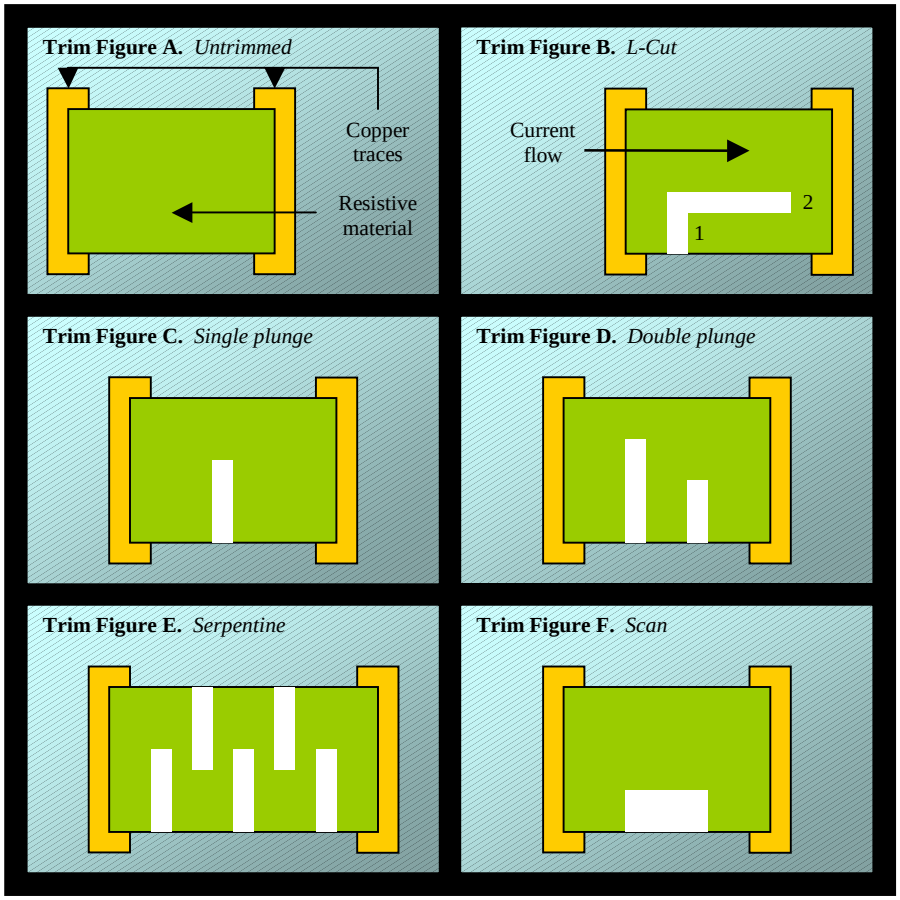


Figure 1.6: Typical embedded resistor trim styles [Fjeldsted *et al.*2002]

Embedded resistor insertion is highly dependent on manufacturing capabilities to pattern and apply in a controllable thickness and physical size competitive with chip resistors. In essence, development goals for buried resistors must enable fabrication sizes

comparable to the smallest discrete resistor and overall tolerance levels consistent with current material stabilities.

Table 1.4: Companies producing embedded resistor material technologies

Company	Technology	Approach
Asahi Kasei Corporation	Carbon paste (polymer thick film)	Subtractive
DuPont	Ceramic (polymer thick film)	Additive
Gould Electronics	Thin metal on copper	Subtractive
Ibiden	Unknown-internal development	
MacDermid	Plated nickel phosphorus	Additive
Multiline International Europea, LP	Carbon paste (polymer thick film)	Subtractive
Mitsui	Thin metal on copper	Subtractive
Omega Technologies	Nickel phosphorus on copper	Subtractive
Shipley	Thin metal on copper	Subtractive

1.3.3 Embedded Capacitors

Justification for the replacement of surface-mount capacitors with embedded capacitors is faster clock speeds. Design issues such as power distribution, impedance, crosstalk, EMI, load distribution and board structure all need to be considered when electronic devices get faster. As a general rule of thumb, when dealing with high speed circuits it is best to place decoupling capacitors as close to an IC as possible. In some cases it makes sense to place capacitors underneath or on top of ICs in order to reduce parasitic inductance. Both situations represent perfect applications for buried capacitors since embedded technologies reduce signal traveling distances.

Capacitors are formed when tow conductive layers are separated by an insulating (dielectric) material (Figure 1.7). When different amounts of voltage are applied to the

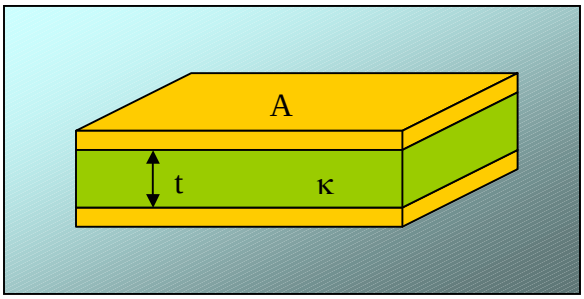


Figure 1.7: Embedded capacitor design

apposing conductive layers, energy is stored within the dielectric material. The amount of energy or capacitance (C) stored is given by Equation 3:

$$C = \frac{\kappa \varepsilon_0 A}{t} \qquad \textbf{(Equation 3)}$$

where,

C = capacitance (F)
κ = dielectric constant
ε_0 = permittivity of free space (8.85×10^{-12} C^2/Nm^2)
A = surface area (m^2)
t = thickness (m)

Currently, there exists a wide variety of dielectric materials available for producing embedded capacitors each of which have many depositing techniques to choose from [Ulrich *et al.*2000]. These materials fall into two main categories: paraelectrics and ferroelectrics. While ferroelectrics have a dielectric constant three orders of magnitude larger than paraelectrics, the stability of paraelectrics's dielectric constant is vastly superior when exposed to operating conditions like temperature, voltage and frequency. In addition, ferroelectrics materials are time sensitive and highly dependent on material conditions like grain size and crystal orientation. In contrast,

paraelectrics are considered amorphous and therefore independent of deposition conditions. Ulrich *et al.*goes into great detail concerning the comparison of paraelectric and ferroelectric materials used for embedded capacitors and provides design rules for choosing theses materials in certain applications [Ulrich *et al.*2000].

Design methodologies for constructing buried capacitors entail embedding electrode patterned dielectric layers within a substrate (Figure 1.8).

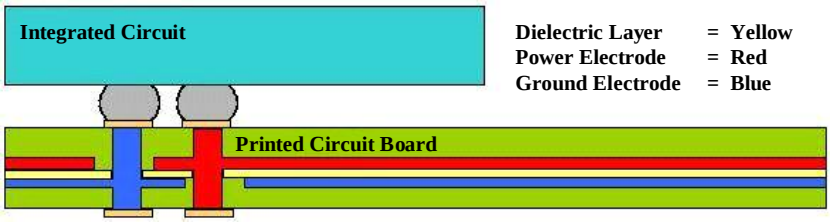


Figure 1.8: Example embedded capacitor design

Various materials used to manufacturer embedded capacitors can be found in Appendix A, Table A.2. Table 1.5 highlights companies involved in embedded capacitor technologies and the materials they manufacture. While embedded resistor design is well defined, capacitor design is not. Embedded capacitor insertion is highly dependent on new material discoveries to provide advances in yield and processibility. In essence, the development goal for buried capacitors is to obtain the highest dielectric constant with the thinnest film in the most reliable form.

Table 1.5: Companies producing embedded capacitor material technologies [Hickman 2003]

Company	Technology
3M	Filled resin (sheet)
Asahi Chemical	Chemical filled paste
Dupont	Filled and unfilled polyimide film/copper
Dupont	Polymer thick film
Dupont	Filled polyimide paste
Hitachi	Chemical filled resin
Ibiden	Unknown-internal development
MicroCoatings	Thin film on dielectric/copper
Mitsui	
Nippon Paint	Filled resin (liquid and sheet)
Sanmina ZBC	Filled resin
Shipley	Thin film on dielectric/copper
Vantico	Filled liquid

1.3.4 Embedded Inductors

Currently, inductors are used in such low quantities that the equivalent per component cost will be too high to incorporate any special processes or materials [Rector 1997]. In addition, since inductors are magnetic devices that benefit from sufficient volumetric space for their magnetic fields to radiate unimpeded, embedding these devices does not make sense for the majority of applications. However, since inductors are usually spirals of conductive material, fabricating them is simply a task of forming a spiral out of an interconnect material with fine line capabilities (Figure 1.9). The inductance of an inductor is given by Equation 4.

Unfortunately, predicting the operating characteristics of a buried inductor is very complex due to the interaction between magnetic fields, the structure's width, spacing, number of turns, inner diameter, spacing to ground and the presence of nearby conductors [Ulrich *et al.*2000]. Therefore, due to the difficulties surrounding accurately modeling

embedded inductors coupled with the permanent nature of embedded technologies, conventional discrete components will most likely be the best design choice for engineers.

Figure 1.9: Embedded inductor design

$$L = \mu N^2 \frac{A}{l} \qquad \textbf{(Equation 4)}$$

where,

L	=	inductance (H)
μ	=	permeability of core medium (Tm/A)
N	=	number of turns
A	=	cross-sectional area (m^2)
l	=	length (m)

1.3.5 Embedded Passive Advantages

Driven by performance, size and economic concerns, embedded passives were introduced to the market in the early 1980s. The potential advantages offered as a result of embedded passives include:

- Increased circuit density through saving real estate on PWB substrates
- Improved electrical properties through additional termination, filtering and shortening electrical connection opportunities
- Cost reduction through increased manufacturing automation
- Increased product quality through the elimination of incorrectly attached devices, and
- Improved reliability through eliminating solder joints

Using embedded passives offers substrate size reduction opportunities. Due to the large number of resistors and capacitors required by traditional, especially analog, circuits, replacement with embedded resistors and capacitors will offer substantial space savings. It is likely that reduction in real estate occupied by passive components will allow many currently double-sided boards to be fabricated with components only on one side, thus decreasing assembly costs. Table 1.6 provides design rules and packaging density forecasts for the hand-held electronic product sector, with projected need for embedded passives beginning in 2001. Referring back to Table 1.2, common characteristics of a few widespread commercial products is available. Likely high

Table 1.6: NEMI roadmap key parameters for hand-held electronic products [NEMI 1996]

Design Packaging Density	1996	1998	2001	2004
Substrate lines and spaces (μm)	100	80	60	30
Substrate pad diameter (μm)	640	300	120	80
Number of components (per cm^2)	4	4.5	5.5	6
Maximum number of components (per cm^2)	23	29	39	54
Passive components (type)	0603	0402	Integral	

volume, high-performance portable applications will realize the benefits from real estate savings due to embedded passive technology first. Figure 1.10 exemplifies the differences between two printed wiring boards (PWBs); the top is constructed using traditional resistors while the bottom one is fabricated using embedded resistors. Visual inspection reveals evident size reduction and accompanying solder joint reduction available through the use of embedded resistors.

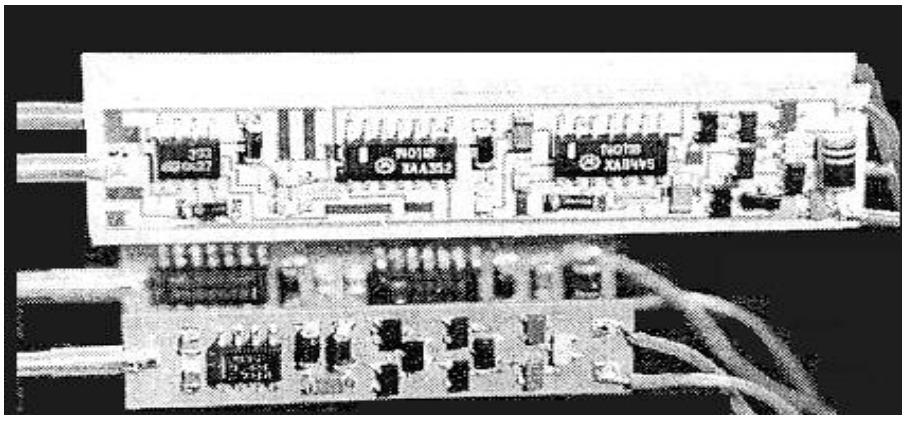


Figure 1.10: Comparison between PWBs using traditional resistors and embedded resistors [DuPont 1998]

Another problem associated with board size is congestion. Applications often require the concentration of multiple passives at a single location on the substrate. If

these situations require discrete passives, the result intensifies routing problems and introduces electrical parasitics which often require custom parts.

Reliability issues with surface-mount discrete capacitors have historically generated some of the biggest concerns for various large automotive electronics suppliers. The shear complexity of the internal structures of these devices predisposes them to failure. Major warranty claims have been linked to solder joint failures and handling damages of the discrete components themselves. Meanwhile, embedded passive technologies will eliminate many of these failure modes. In many cases, chip resistor values are not normally distributed about a mean value resistance. This is a consequence of sorting the as-made resistor population into various tolerance bands. Thus, a sample of 10% tolerance resistors may in fact contain no resistors within 5% of the nominal value. As a result, complications with tolerance stack-up may lead to the purchase of more expensive, tighter tolerance parts than necessary had the distribution been normal. However, this is not the case for embedded passives. Although the strategy for value trimming embedded resistors can be complex and lead to new kinds of skewed distributions, for a minimal additional cost, the strategy can be simple and the results normal. Even though the benefit may seem insignificant, it in fact can enhance the utility of the technology.

1.3.6 Applications

Passive integration is currently being identified by Nokia as a major packaging development for cellular phones and notebook computer applications. Other portable products, such as pagers and hand-held games will also benefit from the use of embedded

passives. Automotives, avionics, medical equipment, wireless local area networks and satellite positioning systems (GPSs) are all also candidates for embedded passives. Recent manufacturers have included passive devices in the following applications:

- Digital electronics for pull-up/pull-down on open collectors for gate inputs
- Line terminations
- LED current limiting
- Switch pad potentiometers and power dividers
- Microwave attenuators
- Parallel and series terminating resistors fabricated into voltage plans of emitter-coupled logic circuitry
- Series terminating resistors for high-speed CMOS applications, and
- Isolation resistors for burn-in boards

Current companies making use of embedded passives include:

Alcatel	Bell
CTS Microelectronics	Cannon
Codex	Concurrent Computer
Control Data Corporation	Cray Research
Data General	Harris Computer
Hewlett Packard	IBM
Intel	Loral Defense
Loral Space	MIPS
Motorola	NCR
National Instruments	National Semiconductor
Nikon	Pentax
Raytheon	Seagate Technology
Sequent Computer	Siemens
Sun Microsystems	

With embedded resistor technology that spans the entire range of resistor values, there is no impediment to the replacement of over 95% of discrete resistors. The only exceptions would be unusually large or small values, very high power distribution requirements or very tight tolerance requirements. The consequences of successful embedded capacitor technology are likely to be less far-reaching in the numbers of discrete passive devices replaced. It will become increasingly difficult to replace large values of capacitance so the replacement of discrete capacitors is unlikely to exceed 50-60%. The projected market share for embedded resistors and capacitors in 2004 is given in Table 1.7.

Table 1.7: Projected market share of embedded resistors and capacitors in 2004 [NEMI 1996]

Application	Projected Market Share in 2004	
	Resistors	Capacitors
Hand Held	64%	58%
High Performance	40%	40%
Cost/Performance	20%	20%
Low Cost	10%	10%
Harsh Environment	20%	20%

1.4 EMBEDDED PASSIVE RELIABILITY ISSUES

1.4.1 Overview

Since embedded passives cannot be tested before being added to a substrate, long term reliability and yield quality are major concerns for designers. As with any backbone of a structure, when the quality of the foundation is poor the entire systems will perform

negatively if at all. While only a few reliability resources exist for embedded passive technologies, information gained from these resources sheds light on operating characteristics and failure modes of embedded passive devices. The major goal for testing embedded passives is to gain knowledge enabling the development of thermally and electrically stable resistive and capacitive materials that can cover a large range of resistive values and high capacitive densities.

1.4.2 Embedded Resistors and Capacitors

One of the key reliability issues for embedded resistors is how well the technology is able to adhere to the surface onto which they are deposited [Ulrich *et al.* 2000]. Furthermore, delaminations between the resistor and copper leads are possible in addition to chemical interactions between resistor and copper electrode materials [Ormet 2001]. Meanwhile, in conjunction with the failure mechanisms listed above, embedded capacitor devices suffer water absorption phenomena bringing concerns governing humidity storage; however, the effects are reversible with simple drying techniques [Croswell *et al.*2002]. These failure modes are a result of manufacturi ng processes and application specific environmental and mechanical loads that subject the embedded resistors and capacitors to large temperature variations and substrate deformations. Testing embedded passive components for these particular failure modes can be achieved through temperature shock, temperature cycling and various bending and torision loading tests [Ulrich *et al.*2000]. J. Zhou, J. Myers and G. Dickenson conducted thermal cycling and electronic shock discharge (ESD) tests on laser trimmed, embedded ceramic paste resistors measuring 100, 1,000 and 10,000 ohms and ceramic capacitors or large and

small sizes buried in FR4 boards [Zhou *et al.* 2001]. No induced failures were observed in any of the tested materials. However, short-comings include: only testing subtractive embedded ceramic paste resistor technologies and not assessing thermal characteristics, long term stability, thermal shocking and humidity exposure. In addition, the sample population did not include reworked embedded resistors, aggregate results were omitted, material stability was assumed upon a subset of a limited sample population and finally, since no failures were observed, subsequent failure mechanisms could not be evaluated. Gould Electronics, Inc. released a white paper reviewing in house reliability assessments of two different types of subtractive thin-film nickel-chromium alloy resistors subject to humidity, thermal cycling, conventional reflow and soldering heat tests [Wang *et al.* 2002]. Short-comings include: only testing subtractive material technologies, laser trimmed and reworked embedded resistors were omitted, and no failure assessment was provided. The effect of power dissipation on embedded thin-film nickel-chromium resistors has been touched upon; however, no environmental qualification was performed [Wang *et al.*2003]. Robert Croswell *et al.* has conducted numerous electrical characterization and environmental and mechanical reliability tests on embedded mezzanine capacitors produced from ceramic-filled photodielectric (CFD) dielectric materials but no embedded resistor technologies were addressed [Croswell *et al.* 2002]. J. Felten *et al.* conducted thermal cycling and ESD testing on ceramic embedded resistors and capacitors as well; however, their research was limited in the same manner as Zhou *et al.* [Felten *et al.* 2001]. Fairchild *et al.* conducted reliability tests on flexible thin-film embedded resistors and electrical characterization of thin-film embedded capacitors and

inductors; however, reworked and laser trimmed embedded resistors were not included within the study [Fairchild *et al.* 1997].

1.5 THESIS OVERVIEW

Chapter 2 documents the conception and methodology governing the composition of the TV-1R test vehicle along with establishing a rigorously accelerated environmental test plan to subject different styles of embedded resistors to in hopes of extracting the operating performance and reliability characteristics of the tested devices. In addition, it explores the experimental techniques, setups and equipment used to perform the test procedures.

Chapter 3 provides the experimental results obtained through each stage of the environmental qualification regimen including: thermal characterization, stabilization baking, thermal cycling, thermal shocking and temperature/humidity aging. In addition, a pre/post lamination analysis was preformed. Furthermore, data analysis methodologies are explored coupled with a material stability assessment and comparison with well-established discrete resistor technologies.

Chapter 4 presents and demonstrates a three stage, hierarchical failure analysis method used to extract the failure mechanisms associated with Gould and MacDermid embedded resistor technologies along with a brief explanation of the equipment used. In addition, a definition of the meaning of failure employed within the scope of this thesis is provided and a summary of the failures caused by each qualification experiment is included.

Chapter 5 provides a summary of the study and draws appropriate conclusions based on the work performed. It then addresses the contributions of the study towards reliability testing of embedded passive technologies and failure assessment of two particular embedded resistor materials/approaches. Finally, present experiments are disclosed and necessary future work is indicated.

CHAPTER 2 TEST VEHICLE AND QUALIFICATION PLAN

2.1 MOTIVATION

For all electronic systems, limitations on the individual component's ability to adhere to specific design criteria, predetermines the characteristics and devices used for an intended application. While the specifications generally differ from application to application, tolerance bands for resistors allow manufactures to decide what devices are available to satisfy their design constraints. Tolerances of ±10% or larger are readily achievable with today's technologies, however, achieving ±1% is a challenge [Fjeldsted *et al.* 2002]. For embedded passives to insert themselves into the mainstream market, performance characteristics and material stability must be comparable to or out perform existing passive technologies. Therefore, long-term operation and storage reliability needs to be assessed for tight tolerance embedded passive components such as embedded resistors.

Chapter 2 focuses on establishing a rigorously accelerated environmental test plan to subject different styles of embedded resistors to in hopes of extracting the operating performance and reliability characteristics of the tested devices. In addition, the primary goal is to acquire an understanding of the particular failure modes that characterize the resistors ability to perform an intended task.

2.2 DESCRIPTION OF TV-1R TEST VEHICLE

2.2.1 Overview

The TV-1R test vehicle is a multi-layer printed wiring board (PWB), approximately 5” square, manufactured from etched FR-406 copper panels designed by Delphi Automotive Systems for the NIST Advanced Embedded Passives Technology Consortium. In order to complete each stage of the fabrication process, the TV-1R board was shipped throughout the United States for selected treatments (Figure 2.1).

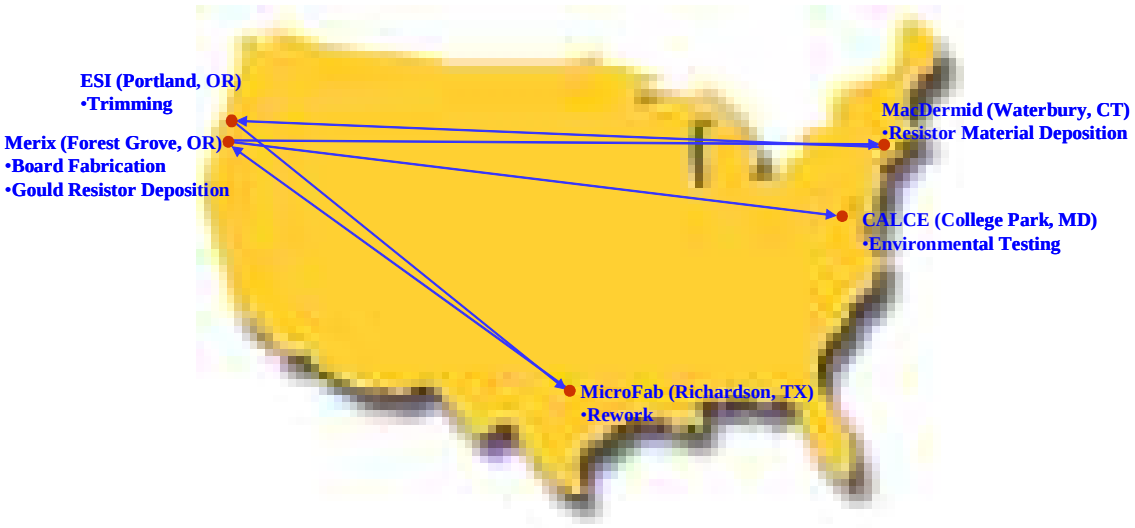


Figure 2.1: Shipping schedule for TV-1R test vehicle

Fabrication of the inner layer pairs and final board lamination was completed by Merix Interconnect Solutions (including resistor material deposition by MacDermid for the additive resistors), while trimming and rework was preformed by Electro Scientific Industries (ESI) and MicroFab Technologies, Inc., respectively. The FR-406 material is an epoxy-glass specifically selected for its characteristic high glass transition temperature

(T_g=170^{o}C) enabling the TV-1R board to withstand severe environmental regimens. Contained within layer 2 of the PWB is an array of 20 cells containing approximately 600 embedded resistors of two distinct material/fabrication approaches described in Section 2.2.2. The 20 cells are equally divided into 10 horizontal and vertical orientations. Figure 2.2 depicts the TV-1R test vehicle with one of the horizontal resistor cells magnified to ease viewing. Note the horizontal resistor orientation runs perpendicular to the edge connector located at the top of the PWB.

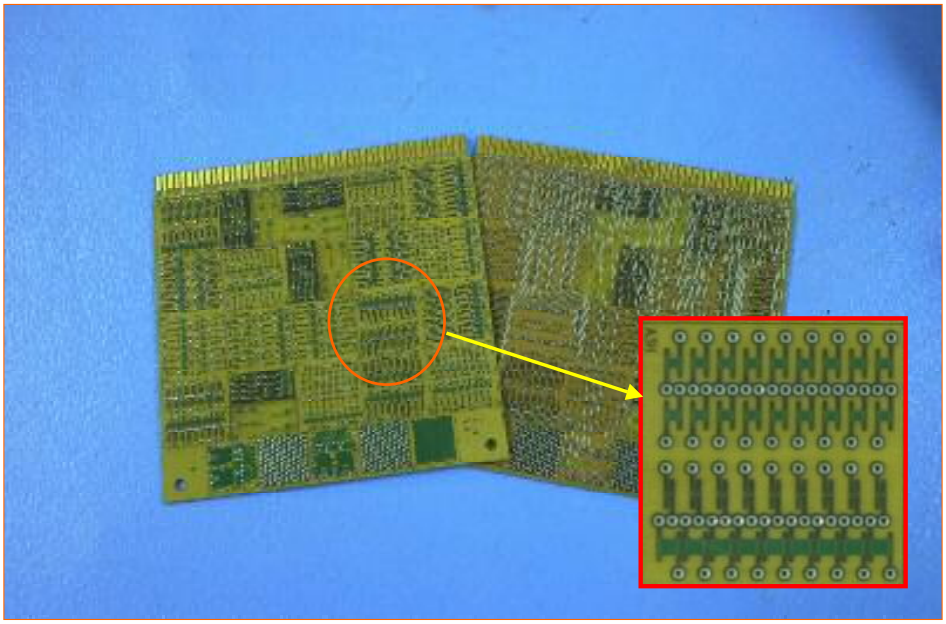


Figure 2.2: TV-1R test vehicle

The TV-1R test vehicle is constructed with only square aspect ratio resistors; however, an assortment of different size resistor squares and IO track widths exist throughout the board. Resistor sizes range from 10 to 50 mils and the IO track widths vary from 5 to 20 mils. Cell arrangements contain two distinctive internal patterns, either

a daisy chained configuration consisting of 4 strings of 9 resistors (36 resistors in total) or a combination of daisy chained and isolated resistor configurations. At the top of the PWB resides a 100 contact edge connector provided for testing purposes of selected resistor terminations; either daisy chained or isolated resistor configurations. Table 2.1 contains the corresponding test-point resistor pin-out for the TV-1R board. Furthermore, resistors have been trimmed and selected resistors are reworked according to the processes described in Sections 2.2.3 and 2.2.4.

Table 2.1: TV-1R resistor pin-out

Pin Descriptor	Mating Pin Descriptor	Edge Connector Pin #	Mating Edge Connector Pin #	Test Pattern Description
A0H	GND1	81	55	Daisy Chain, 20 mil runner, 5,30,30,50 mil gaps
A0V	GND1	3	55	Daisy Chain, 20 mil runner, 5,30,30,50 mil gaps
A1H	GND1	39	55	Daisy Chain, 10 mil runner, 5,30,30,50 mil gaps
A1V	GND1	59	55	Daisy Chain, 10 mil runner, 5,30,30,50 mil gaps
A2H	GND1	35	55	Daisy Chain, 5 mil runner, 5,30,30,50 mil gaps
A2V	GND1	2	55	Daisy Chain, 5 mil runner, 5,30,30,50 mil gaps
A3H-1A	A3H-1B	31	25	Isolated, 30 mil gap, 20 mil runner
A3H-2A	A3H-2B	30	24	Isolated, 30 mil gap, 20 mil runner
A3H-3A	A3H-3B	23	20	Isolated, 5 mil gap, 20 mil runner
A3H-4A	A3H-4B	27	18	Isolated, 55 mil gap, 20 mil runner
A3V-1A	A3V-1B	1	4	Isolated, 55 mil gap, 20 mil runner
A3V-2A	A3V-2B	5	9	Isolated, 5 mil gap, 20 mil runner
A3V-3A	A3V-3B	8	15	Isolated, 30 mil gap, 20 mil runner
A3V-4A	A3V-4B	14	19	Isolated, 30 mil gap, 20 mil runner
A4H-1	GND1	52	55	Isolated, 30 mil gap, Cu/poured Cu
A4H-2	GND1	54	55	Isolated, 30 mil gap, Cu/poured Cu
A4H-3	GND1	51	55	Isolated, 5 mil gap, Cu/poured Cu
A4H-4	GND1	53	55	Isolated, 55 mil gap, Cu/poured Cu
A4H-5	A4H-6	41	38	Isolated, 30 mil gap, no Cu
A4H-7	A4H-8	42	45	Isolated, 5 & 55 mil gap, no Cu
A4V-1	GND1	89	55	Isolated, 30 mil gap, Cu/poured Cu
A4V-2	GND1	70	55	Isolated, 30 mil gap, Cu/poured Cu
A4V-3	GND1	68	55	Isolated, 5 mil gap, Cu/poured Cu
A4V-4	GND1	56	55	Isolated, 55 mil gap, Cu/poured Cu
A4V-5	A4V-6	90	71	Isolated, 30 mil gap, no Cu

Pin Descriptor	Mating Pin Descriptor	Edge Connector Pin #	Mating Edge Connector Pin #	Test Pattern Description
A4V-7	A4V-8	72	63	Isolated, 5 & 55 mil gap, no Cu
B0H	GND1	34	55	Daisy Chain, 20 mil runner, 10,20,40,50 mil gap
B0V	GND1	100	55	Daisy Chain, 20 mil runner, 10,20,40,50 mil gap
B1H	GND1	7	55	Daisy Chain, 10 mil runner, 10,20,40,50 mil gap
B1V	GND1	29	55	Daisy Chain, 10 mil runner, 10,20,40,50 mil gap
B2H	GND1	83	55	Daisy Chain, 5 mil runner, 10,20,40,50 mil gap
B2V	GND1	97	55	Daisy Chain, 5 mil runner, 10,20,40,50 mil gap
B3H-1A	B3H-1B	92	91	Isolated, 20 mil runners, 10 mil gap
B3H-2A	B3H-2B	94	93	Isolated, 20 mil runners, 50 mil gap
B3H-3A	B3H-3B	99	96	Isolated, 20 mil runners, 40 mil gap
B3H-4A	B3H-4B	95	98	Isolated, 20 mil runners, 20 mil gap
B3V-1A	B3V-1B	22	13	Isolated, 20 mil runners, 20 mil gap
B3V-2A	B3V-2B	26	21	Isolated, 20 mil runners, 40 mil gap
B3V-3A	B3V-3B	32	28	Isolated, 20 mil runners, 50 mil gap
B3V-4A	B3V-4B	36	33	Isolated, 10 mil runners, 50 mil gap
B4H-1	B4H-2	64	65	Isolated, 5 mil runner, 50 mil gap, no Cu
B4H-3	B4H-4	66	67	Isolated, 5 mil runner, 40 & 20 mil gap, no Cu
B4H-5	GND1	75	55	Isolated, 5 mil runner, 20 & 50 mil gap, Cu/poured Cu
B4H-6	GND1	76	55	Isolated, 5 mil runner, 40 mil gap, Cu/poured Cu
B4H-7	GND1	77	55	Isolated, 5 mil runner, 50 mil gap, Cu/poured Cu
B4H-8	GND1	82	55	Isolated, 5 mil runner, 10 mil gap, Cu/poured Cu
B4V-1	B4V-2	46	37	Isolated, 5 mil runner, 40 & 20 mil gap, no Cu
B4V-3	GND1	40	55	Isolated, 5 mil runner,20 mil gap, Cu/poured Cu
B4V-4	B4V-7	48	57	Isolated, 5 mil runner,10 & 50 mil gap, no Cu
B4V-5	GND1	49	55	Isolated, 5 mil runner,40 mil gap, Cu/poured Cu
B4V-6	GND1	50	55	Isolated, 5 mil runner,50 mil gap, Cu/poured Cu
B4V-8	GND1	58	55	Isolated, 5 mil runner,10 mil gap, Cu/poured Cu

Pin Descriptor	Mating Pin Descriptor	Edge Connector Pin #	Mating Edge Connector Pin #	Test Pattern Description
DH-1	GND1	12	55	10 mil tapered
DH-2	GND1	16	55	5 mil serpentine
DH-3	GND1	17	55	20 mil straight
DH-4	GND1	43	55	10 mil serpentine
DH-5	GND1	44	55	10 mil straight
DH-6	GND1	47	55	20 mil tapered
DH-7	GND1	60	55	5 mil tapered
DH-8	GND1	62	55	20 mil serpentine
DH-9	GND1	61	55	5 mil straight
DV-1	GND1	87	55	10 mil tapered
DV-2	GND1	88	55	5 mil serpentine
DV-3	GND1	85	55	20 mil straight
DV-4	GND1	84	55	10 mil serpentine
DV-5	GND1	79	55	10 mil straight
DV-6	GND1	80	55	20 mil tapered
DV-7	GND1	78	55	5 mil tapered
DV-8	GND1	73	55	20 mil serpentine
DV-9	GND1	74	55	5 mil straight
ECOMB	GND1	6	55	Comb Pattern to GND, 10/10 & 15/15 line/space
GND1		55		Ground + Poured copper on B4V
GND2		10		Ground
GND3		11		Ground
GND4		69		Ground
NC		86		No Connection

2.2.2 Embedded Resistor Approaches

Two distinctive types of embedded resistor materials/approaches, provided by Gould Electronics and MacDermid Incorporated, were fabricated into the TV-1R test vehicle. The MacDermid M-Pass™ nickel phosphorous (NiP) material is plated directly onto the inner layer pairs of the FR-406 PWB through an additive process. Meanwhile, Gould uses a dedicated layer pair in conjunction with a subtractive technique starting with a copper foil coated with resistive nickel chromium (NiCr) material that requires a multi-stage photoresist and etching process to fabricate the required pattern. The buildup of the two types of resistors is illustrated in Figure 2.3.

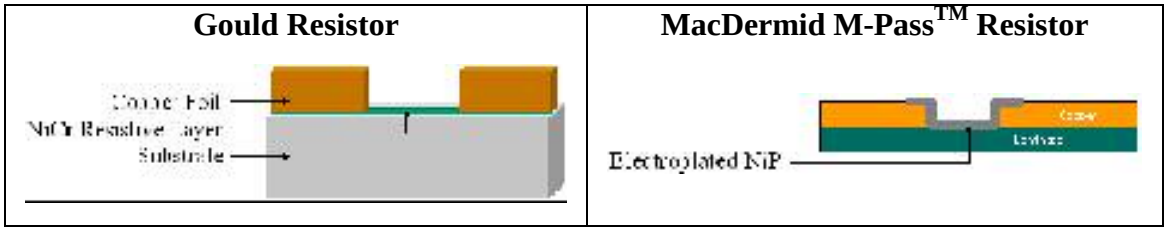


Figure 2.3: Gould and MacDermid embedded resistor buildup

Both embedded resistor materials have the ability to be trimmed and/or reworked prior to board lay up and lamination. Using a laser trimming process, manufacturers are able to fabricate a wide range of resistor values through shaped cuts in the resistive material described earlier in Chapter 1. Trimming increases the resistance to enable manufacturers to initially fabricate the resistors with a lower than required value. Similarly, resistance values may be reduced in magnitude by an ink-jet printing process

which deposits a conductive polymer ink in small, controlled size droplets over the surface of the resistor in a rework process.

2.2.3 Trimming Process

For many years, manufactures have preformed laser trimming processes to increase resistance values for film resistors on silicon and surface mount discrete resistors prior to packaging [Berry *et al.* 1968]. However, only recently, have highly automated laser trimming technologies been developed and demonstrated to reliably trim embedded resistors during the board fabrication process [Fjeldsted *et al.* 2002]. Prior to lamination, the inner layers containing deposited resistors are attached to a jig and fed into a laser trim machine programmed with each individual resistor's coordinates. Generally, resistors are trimmed by micromachining a plunge (trench) into a resistive element. The resulting length and path-shape of the plunge determines the resistance change obtained. Several different path-shapes are used depending on the specific trimming requirements (Figure 1.6). In order to manage the process, the resistor's value is measured and feed back to a control system as the laser cuts into the element. Once the desired value is obtained, the laser moves onto the next component until the entire board is complete.

Electro Scientific Industries (ESI) conducted the embedded resistor trimming process for the TV-1R test vehicle. Figure 2.4 depicts ESI's embedded passive component laser trimming system and a magnified view of a laser trimmed, buried resistor. Meanwhile, Table 2.2 provides the cell locations on the TV-1R containing trimmed resistors.

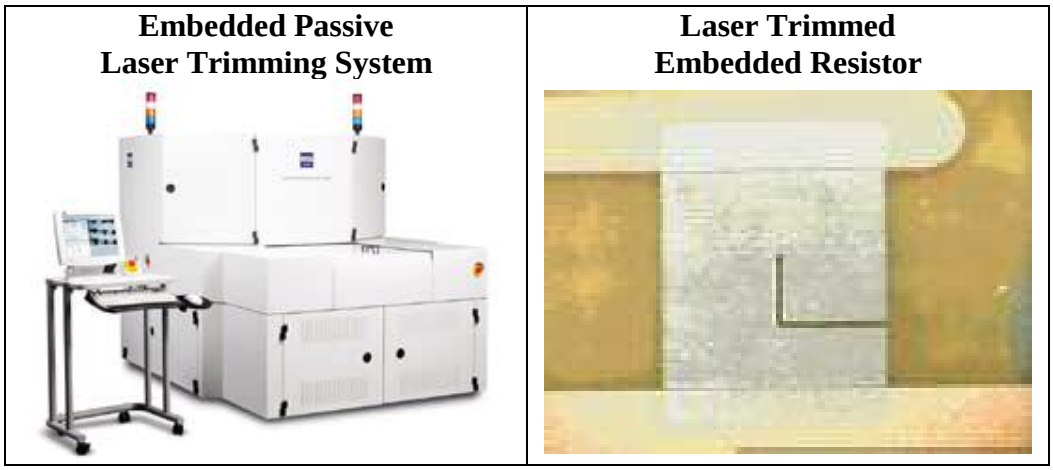


Figure 2.4: ESI embedded passive component laser trimming system [ESI]

Table 2.2: Proposed Cell Locations for Trimmed Resistors

Cell ID	Configuration
A0V	Vertical Daisy Chain
A1V	Vertical Daisy Chain
A2V	Vertical Daisy Chain
A3V	Vertical Isolated
A4V	Vertical Isolated
B0V	Vertical Daisy Chain
B1V	Vertical Daisy Chain
B2V	Vertical Daisy Chain
B3V	Vertical Isolated
B4H	Horizontal Isolated

2.2.4 Rework Process

Generally, reworking embedded resistors is done to correct high resistance values induced by trimming errors (over trimming), material inconsistencies and/or manufacturing defects developed during the PWB fabrication process. One method to rework buried resistors entails printing a conductive ink on the surface of the device to produce a parallel resistor that effectively "trims down" the resistor's value [Shah *et al.*

2002]. Two approaches are used to ink-jet print polymer materials onto resistors for rework. In "Continuous, Charge and Defect" ink-jet printing, fluid under pressure released from an orifice breaks into uniform droplets, electrically charged, by the amplification of capillary waves induced onto a jet [Pimbley 1984]. The drops' location is controlled by the reaction of charges between the droplets and a generated deflection field. Droplets can be generated up to 0.5mm in diameter. Generally this process is suitable for high-speed deposition onto large areas [Virang *et al.*2002]. The other approach called "Drop-On-Demand" (DOD) restricts droplet ejection through a voltage controlled transducer that produces drops approximately equal to the orifice diameter of the generator [Wallace 1989]. Drops can be generated varying from 20 to 100µm. Figure 2.5 illustrates the two ink-jet printing processes.

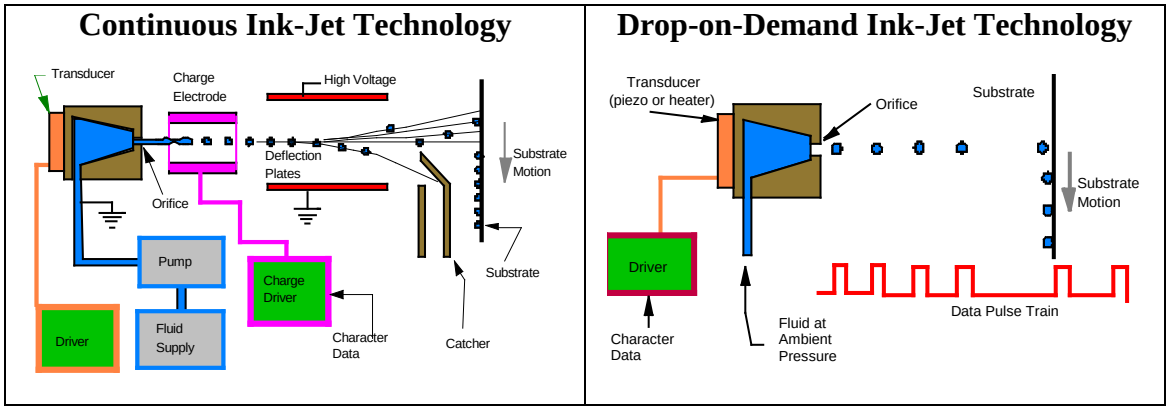


Figure 2.5: Ink-jet printing technologies used for resistor rework

MicroFab Technologies, Inc. performed the embedded resistor rework for the TV-1R test vehicle using a proprietary conductive polyimide based ink used to lower individual resistance values. A custom-made substrate holder was designed to

accommodate 12”x18” PWB inner layer panels for the TV-1R board. Figure 2.6 depicts the Jetlab® DOD ink-jet printing platform and a close up of the TV-1R inner layer panel mounted on a heated aluminum platen thermally isolated by four Vespel standoffs. Table 2.3 provides the design matrix for the TV-1R locating trimmed and/or/neither reworked embedded resistor cells.

Figure 2.6: MicroFab DOD Ink-jet printing machines [Shah *et al.*2003]

Table 2.3: TV-1R Design Matrix[1]

Cell ID	Orientation	Trimmed	Reworked	Final Configuration	
A0V	V	X		D	T
A0H	H		X	D	R
A1V	V	X	X	D	TR
A1H	H			D	N
A2V	V	X		D	T
A2H	H		X	D	R
A3V	V	X		I	T
A3H	H		X	I	R
A4V	V	X	X	I	TR
A4H	H			I	N
B0V	V	X		D	T
B0H	H		X	D	R
B1V	V	X	X	D	TR
B1H	H			D	N
B2V	V	X	X	D	TR
B2H	H			D	N
B3V	V	X		I	T
B3H	H		X	I	R
B4V	V			I	N
B4H	H	X	X	I	TR
H = Horizontal V = Vertical		D = Daisy Chain I = Isolated	R = Reworked T = Trimmed	TR = Both N = Neither	

[1] Due to a manufacturing mistake on the part of Electro Scientific Industries, all resistor cells were trimmed instead of adhering to the TV-1R design matrix.

2.3 QUALIFICATION TEST PLAN

2.3.1 Overview

Twenty-seven printed wiring boards of each type of embedded resistor material (54 boards in total) were fabricated and available to the environmental qualification test regimen. All of the qualification experiments were conducted within the Computer Aided Life Cycle Engineering (CALCE) Electronic Products and Systems Center Environmental Testing Laboratory at the University of Maryland at College Park according to the outlined process flow diagram illustrated in Figure 2.7. Note, the numbers located between arrow paths reveal the amount of each type of board subjected to the proceeding experiment. Testing commenced with initial metrology to determine baseline resistance values. Then, 2 boards of each type, 4 boards total, were used to establish upper and lower bound temperatures of both the TV-1R PWB test samples and the environmental simulation chambers. Then, subsets of samples (5 boards of each type, 10 boards total) were subjected to linearly increasing temperature; stabilization bake, thermal shock, temperature cycling and temperature/humidity accelerated aging profiles. During predetermined, periodical time intervals, the TV-1R boards were measured to extract test point resistance values. Finally, after running each of the qualification tests subsequent data and failure analysis was performed on the test samples to determine material stability, operating performance, reliability attributes and failure mechanisms characteristic to Gould's subtractive NiCr and MacDermid's additive NiP laser trimmed and/or/neither reworked embedded resistors in daisy chained or isolated configurations, oriented horizontally or vertically in various size resistive elements and I/O tracks.

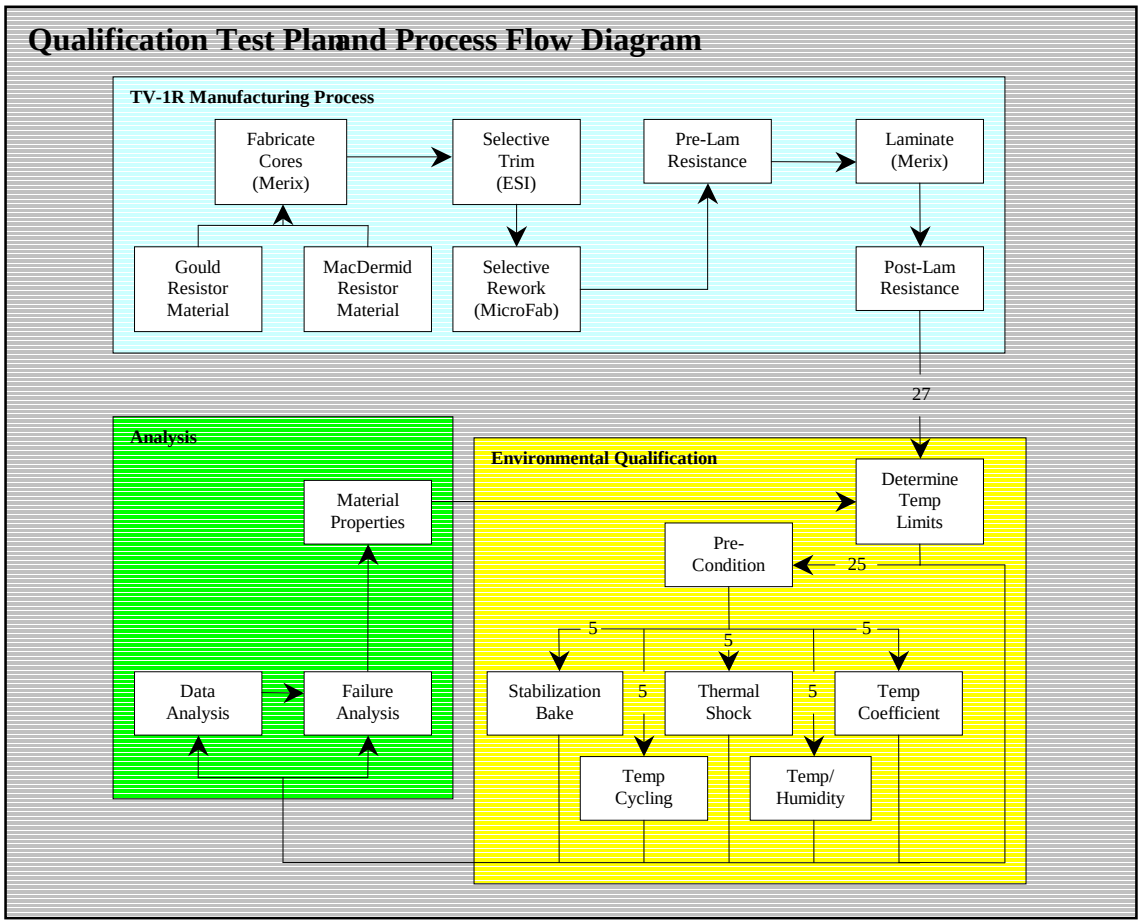


Figure 2.7: Qualification Process Flow Diagram

The pre-conditioning stage was eliminated from the qualification test plan in order to avoid initial resistor damage and thus remove an unnecessary unknown parameter, combinatory effects between qualification tests and preconditioning profiles. If an additional set of TV-1R boards were available, it would have been beneficial to conduct another series of experiments with pre-conditioned test vehicles subjected to a reflow profile to simulate a full electronic system manufacturing process before environmental qualification commenced.

2.3.2 Data Acquisition

Periodic resistance measurements were performed with Agilent's 34970A Data Acquisition/Switch Unit loaded with 3, 20 channel plug-in multiplexers providing 60 possible measurements (Figure 2.8). Figure 2.9 illustrates the computer/test vehicle interface used to store acquired data into excel spreadsheets.

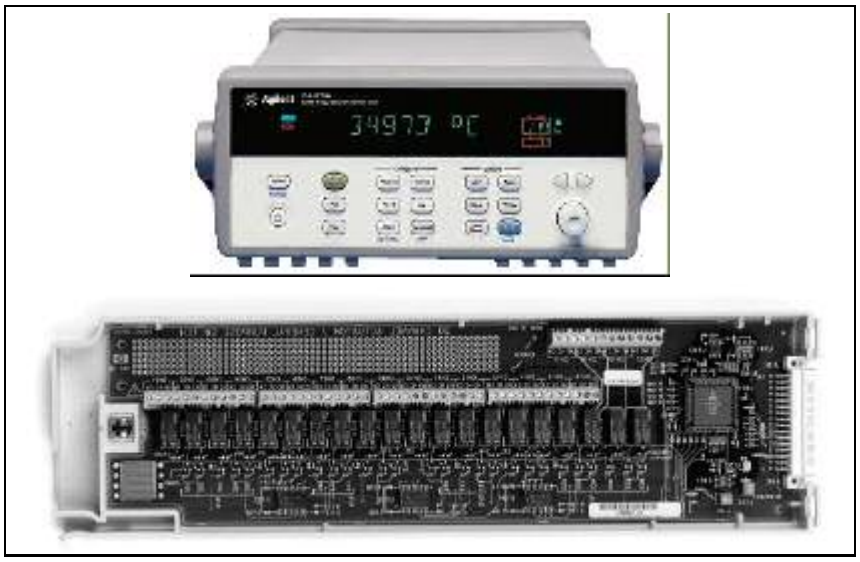


Figure 2.8: Agilent 34970A Data Acquisition/Switch Unit (above) 20 channel multiplexer (below)

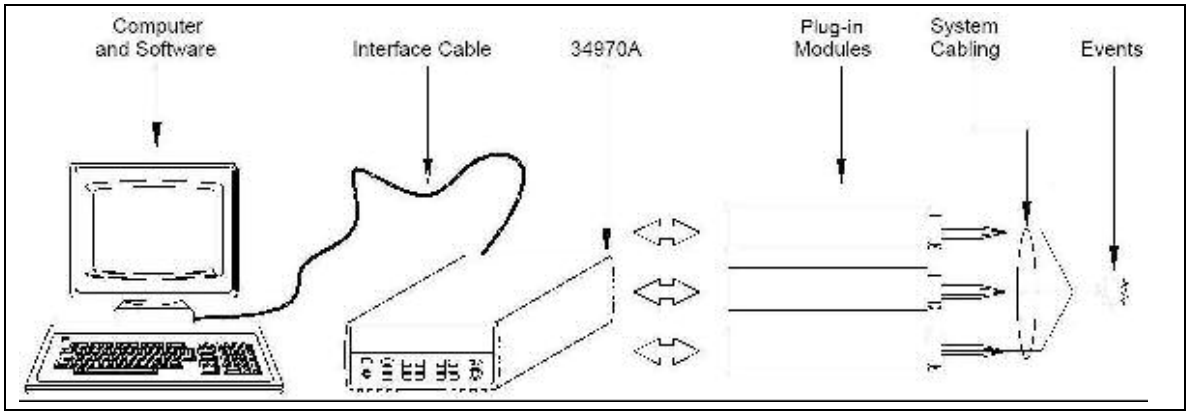


Figure 2.9: Computer, data logger and test vehicle interface

An RS-232 cable was used between the computer and data logger while a custom built 60-pin male/female connector linked the data logger to a 100-pin connector attached to the TV-1R test vehicle's 100 contact edge connector. The test setup enabled 6.5 digits (22 bits) of resolution and less than 1% error.

2.3.3 Environmental Simulation Chambers

In order to accelerate testing conditions, four environmental simulation chambers were used. Table 2.4 lists each of the qualification experiments and the corresponding environmental chamber employed while Table 2.5 provides the testing capabilities of each chamber.

Table 2.4: Environmental Simulation Chambers

Qualification Test	Environmental Simulation Chamber
Temperature Coefficient of Resistance	ESPEC PRA-3AP
Stabilization Bake	ESPEC PRA-3AP
Temperature Cycling	BMA TC-4
Thermal Shock	ESPEC TSB-5
Temperature/Humidity	ESPEC HAST TPC-412M

Table 2.5: Simulation Capabilities

Simulation Chamber	Temperature Range (^{o}C)	Cooling (^{o}C/min)	Heating (^{o}C/min)	Relative Humidity Range (%)	Working Volume (ft^3)
ESPEC PRA-3AP	-20-150	1	2.5	0-98	8
BMA TC-4	-73-220	25	5	N/A	4
ESPEC TSB-5	Low: -65-0 High: 70-200	N/A	N/A	N/A	0.16
ESPEC HAST TPC-412M	105-162	1	1	75-100	0.7

2.4 ENVIRONMENTAL QUALIFICATION TEST PROCEDURES

2.4.1 Thermal Characteristics

To determine the temperature coefficient of resistance (TCR), test samples were subjected to the thermal profile illustrated in Figure 2.10. Over a 4 hour time period, resistance measurements were taken every minute while the temperature linearly increased from -25°C to 125°C.

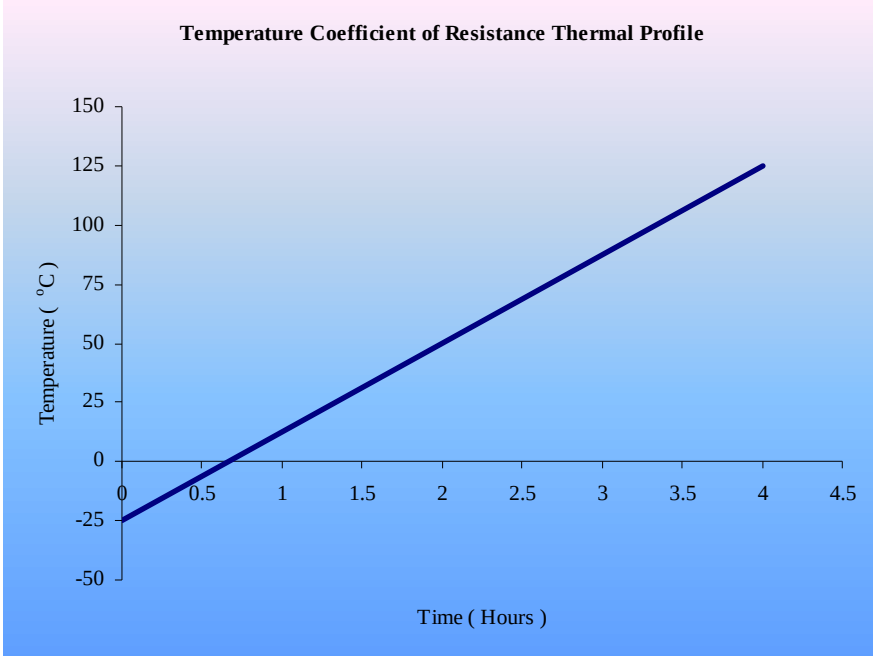


Figure 2.10: Temperature coefficient of resistance thermal profile

2.4.2 Stabilization Bake

To determine the sensitivity of the TV-1R test vehicle to storage at elevated temperatures without electrical stress applied, a stabilization bake at 105°C for 2400

hours was performed. The qualification experiment was modeled after test scheme MIL-STD-883E Method 1008.2. During periodic intervals, initially starting at 24 hours and gradually growing to 100 hours, the test samples were removed from the environmental chamber and measured for resistance at ambient temperature. Although the qualification test necessitates a constant temperature, having to remove the samples from the chamber and cool them to ambient temperature introduced the TV-1R boards to slight temperature cycling effects.

2.4.3 Temperature Cycling

The temperature cycling profile was modeled after test scheme MIL-STD-883E Method 1010.7 to determine the resistance of the TV-1R test vehicle to extremes of high and low temperatures and the effect of alternate exposures to those extremes. The exact thermal profile is illustrated in Figure 2.11. Low pressure liquid nitrogen, controlled through a 50psi pressuring valve, was employed to cool the air temperature in the BMA TC-4 environmental chamber. The test samples, initially at ambient temperature, were ramped up at 5^{o}C/min to 125^{o}C, allowed to dwell for 30 minutes, then ramped down to -65^{o}C to dwell again and finally ramped back up to ambient temperature. The qualification plan specified a total of 500 cycles conducted in 10 cycle intervals at which resistance measurements were taken at ambient temperature. Although the thermal profile exhibits sharp corners at the conclusion of each ramping portion of the experiment, due to the effects of thermal equilibrium, the realized profile would observe more curvature resulting in slightly diminished dwell times.

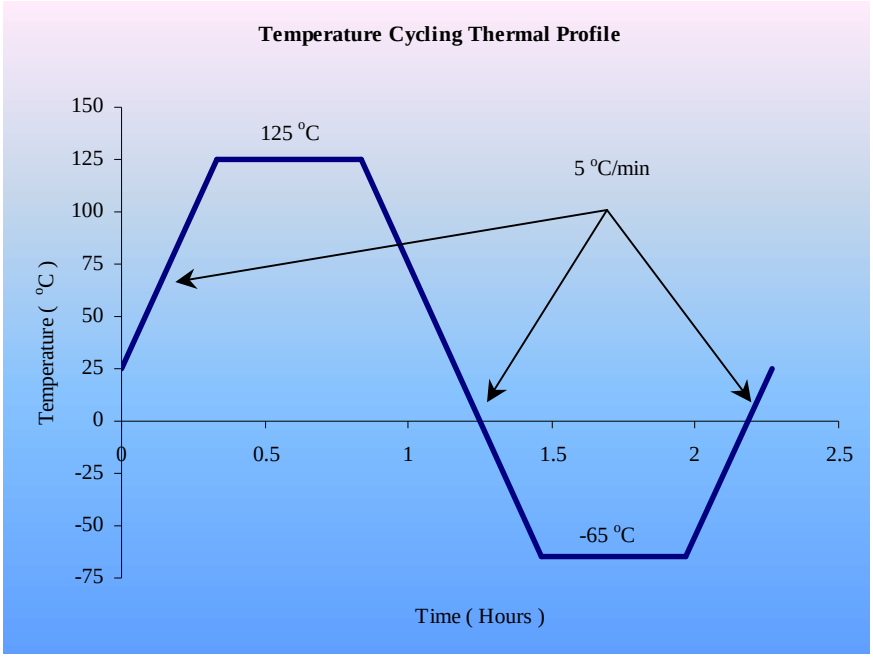


Figure 2.11: Temperature cycling thermal profile

2.4.4 Thermal Shock

Liquid-to-liquid thermal shocks were modeled after test scheme MIL-STD-883E Method 1011.9 in order to determine the sensitivity of the TV-1R test vehicle to sudden exposure to extreme changes in temperature and the effect of alternate exposures to those extremes. The actual temperature profile is illustrated in Figure 2.12. Both low and high temperature thermal shock baths contained Galden D02 low molecular weight perfluoropolyether (PFPE) fluid, heated and cooled by the ESPEC TSB-5 thermal shock chamber. The test samples, initially at ambient temperature, where dipped into a 120^{o}C bath, allowed to dwell for 5 minutes, then immediately transferred and dipped into a -40^{o}C bath to dwell for another 5 minutes and finally removed to ambient temperature.

The qualification plan specified a total of 500 cycles conducted in 10 cycle intervals at which resistance measurements where taken at ambient temperature. Although the temperature profile exhibits a step function, due to minute transfer times between baths and the effects of thermal equilibrium, the realized profile would observe a more curvaceous, sinusoidal resembling profile resulting in slightly diminished dwell times.

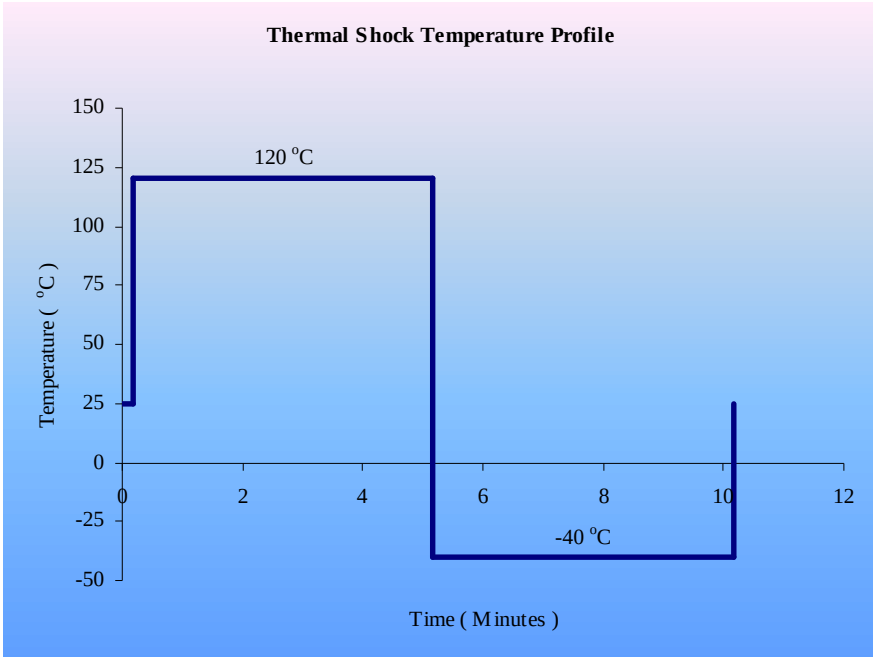


Figure 2.12: Thermal shock temperature profile

2.4.5 Temperature/Humidity

Temperature/humidity accelerated aging was modeled after test method JESD22-A110-B to determine the reliability characteristics of the TV-1R test vehicle to humid environments. Thermal conditions entailed pressurizing the samples under 2.325atm at

130°C with 85% relative humidity for 1000 hours, although 1244 hours were performed. According to the EIA/JEDEC standard, this level of stress usually activates the same failure mechanisms as the "85/85" Steady-State Humidity Life Test (JEDEC Standard No. 22-A101) but at an accelerated rate [EIA/JEDEC 1999]. In order to achieve the specified test conditions, a highly accelerated temperature and humidity stress test chamber (HAST chamber) was necessary. Figure 2.13 illustrates the configuration of a typical HAST chamber. During periodic intervals, initially starting at 24 hours and gradually growing, the test samples were acquisitioned for resistance measurements at ambient temperature. Although the qualification test specifies a constant temperature and relative humidity, having to remove the samples from the HAST chamber and cool them to ambient temperature introduced the TV-1R boards to slight temperature cycling effects and a short duration of time where water was allowed to escape back into the atmosphere from the PWB test vehicles.

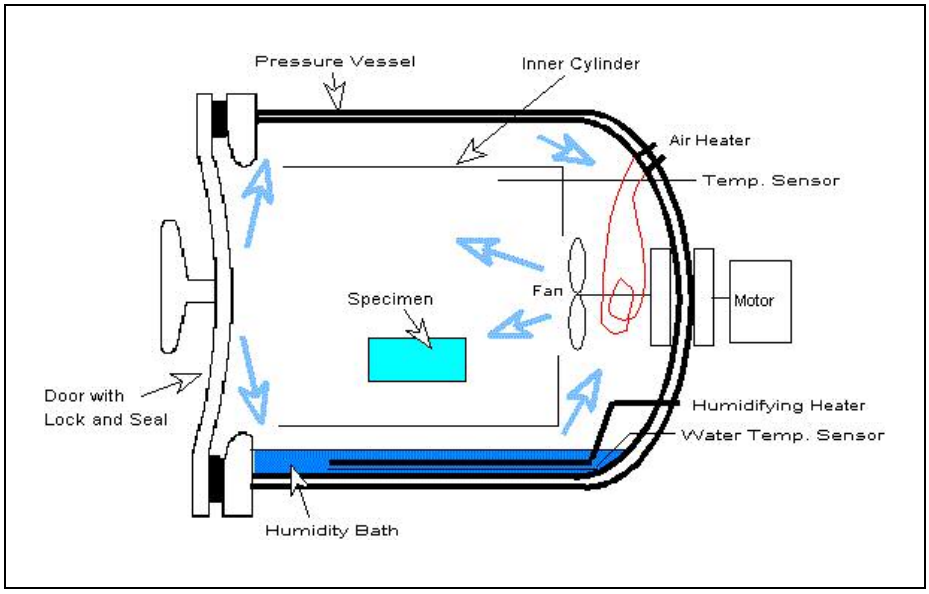


Figure 2.13: HAST chamber configuration [ESPEC]

CHAPTER 3 EXPERIMENTAL RESULTS

3.1 INTRODUCTION

3.1.1 Overview

Chapter 3 focuses on illustrating and discussing the experimental results obtained through the accelerated environmental qualification regimen applied to the TV-1R test vehicles. Each experiment was conducted as described by the reliability test plan presented earlier in Chapter 2. Before any testing commenced, every TV-1R PWB was tested for initial baseline resistance values. Then, each board subjected to a particular environmental reliability experiment was periodically re-tested as prescribed in the appropriate test procedure. Finally, the acquired data was grouped and sorted according to individual embedded resistor characteristics (technology, rework, connection and orientation) in order to generate suitable time-dependent and statistical representations presenting aggregate resistance fluctuation within the sample population. Subsequent data analysis was performed employing Microsoft Excel spreadsheets.

3.1.2 Statistical Representation

In order to present all of the acquired embedded resistor results in a compact fashion, histograms were generated for each of the qualification experiments on the basis of initial baseline and final stressed resistor measurements. For all of the tests except the thermal characterization regimen, this meant calculating a percent difference in resistance for each test location. A percentage increase designates an increase in resistance while a decrease reflects a decrease in resistance. In addition, vertical lines were inserted into

each histogram to represent zero change in resistance or a null effect. Meanwhile, vertically boxed regions above the x-axis were included to designate distribution locations where time-dependent resistor variations were analyzed whereas horizontally boxed regions below the x-axis assign intervals over which a histogram was magnified to investigate possible shifts in the location of peak of the distribution. Furthermore, the total number of data points (data count) used to create a histogram appears in the upper left hand corner of each distribution representing the total amount of measured embedded resistor quantities plotted within the diagram whether they were configured in an isolated or daisy chained fashion. Therefore, except for the pre/post lamination figures, data counts should not be mistaken for the total number of resistor values plotted. In the same manner, each probability density function characterizes the likelihood of a percent change attributable to a measurement and not a single resistor. Justification for combining isolated and daisy chained measurements into single data counts was the result of analyzing each environmental qualification test's data sorted into isolated and daisy chained configurations. Since practically no quantifiable shift occurred in any portion of the distributions as a result of segregating the data, only combined isolated and daisy chained resistor results are represented in the proceeding histograms. As a consequence, each generated probability density function can also be interpreted as the likelihood of a single resistor or a daisy chain of resistors to change value by a particular amount. A representative example from the temperature shock qualification experiment is illustrated in Figure 3.1 demonstrating the lack of sensitivity to isolated and daisy chained configurations with respect to the peak interval.

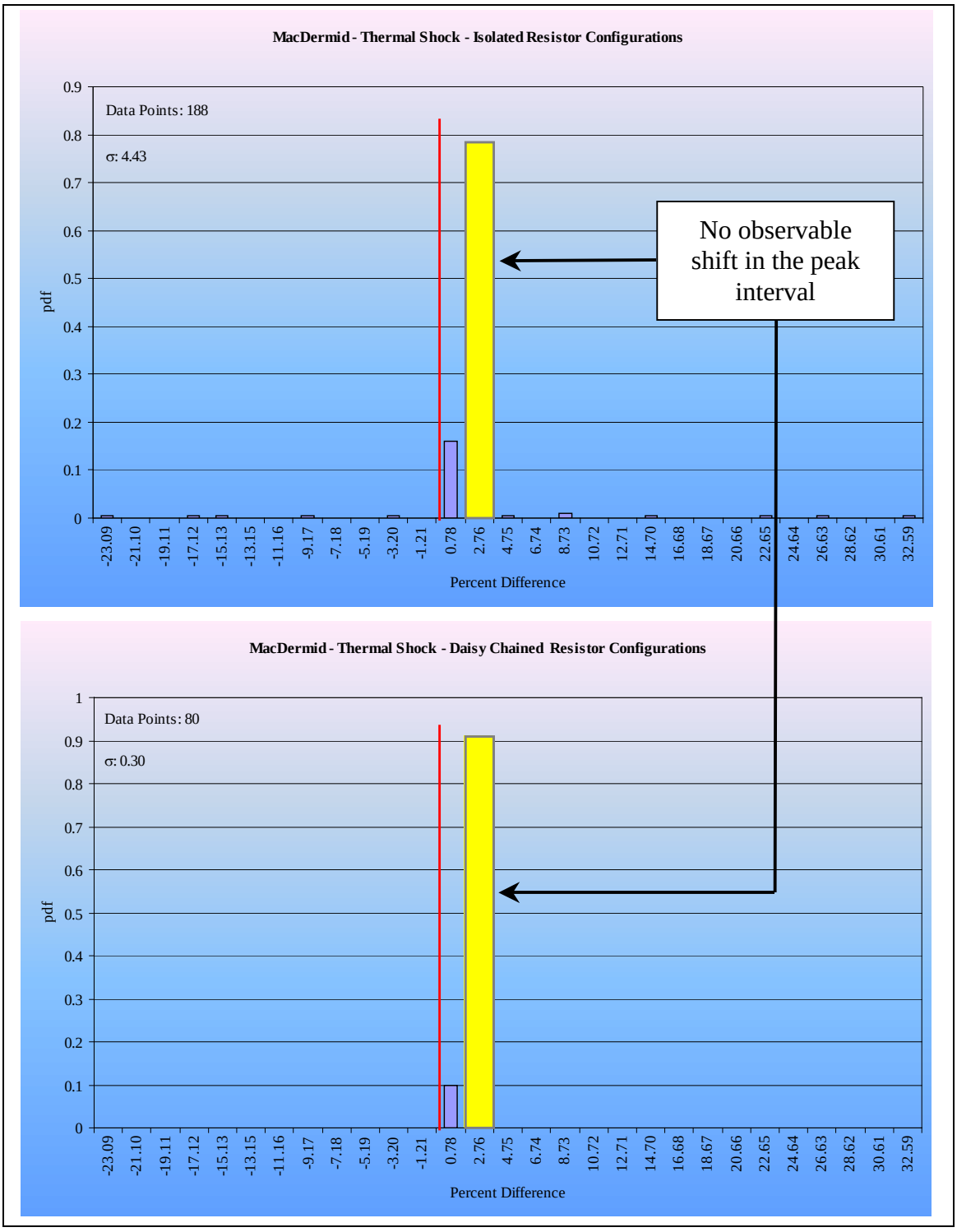


Figure 3.1: Segregation of thermally shocked isolated and daisy chained embedded resistors

3.1.3 Time-Dependent Representation

To properly characterize both Gould and MacDermid embedded resistor technologies, a mutual understanding governing the static as well as the dynamic behavior of the resistor must be known. Since trend data demonstrates dynamic behavior over time, time-dependent plots conveying dynamic resistance fluctuation are included for each of the qualification experiments in addition to the histograms presenting static final resistance change. Figure 3.2 illustrates the locations within a generated distribution where three embedded resistors were inspected for time-dependent trends. One resistor was selected from the peak of the distribution, and two resistors were selected from the left and right extremes[2].

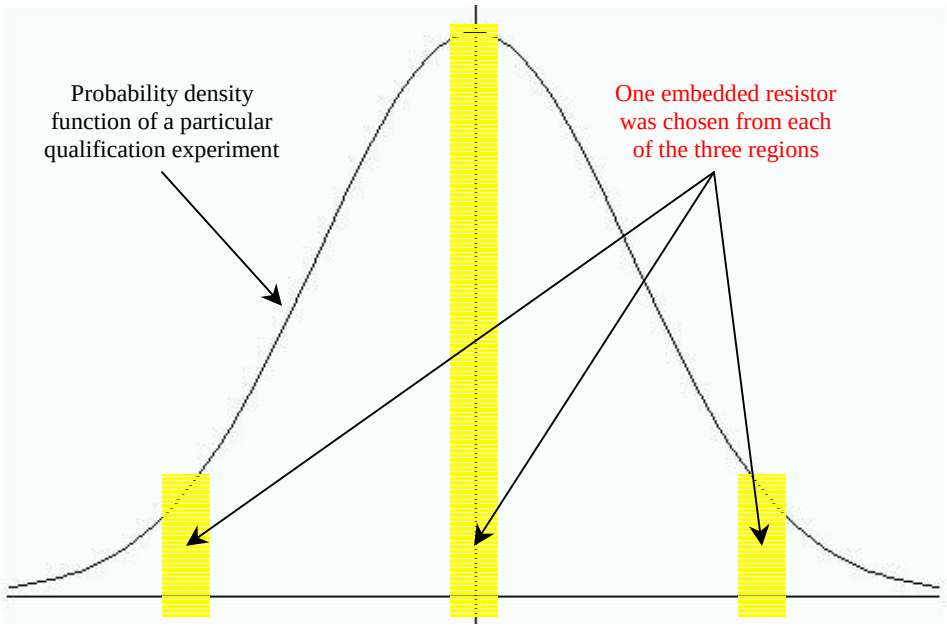


Figure 3.2: Locations of resistors selected for time-dependent representation

[2] Left and right extreme case resistors will be plotted together with the left extreme plotted on the left axis scale and right extreme plotted on the right axis scale, see Figure 3.4.

3.2 PRE/POST LAMINATION ANALYSIS

In order to determine the effect on the embedded resistors due to the PWB lamination process, each individual resistor was measured before and after the layer pairs were press laminated together. Measurements were made by Merix Incorporated using a flying probe to extract resistance values between plated through holes located before and after each of the embedded resistors. Figure 3.3 presents aggregate resistance fluctuation for both Gould and MacDermid resistor technologies. Data counts residing at the top of each figure portray the amount of resistors plotted. Outliers were eliminated on the basis of single occurrences unquestionably uncharacteristic of the rest of the distribution. In most cases, outliers exhibited percent change values far exceeding 1000% and can possibly be attributed to manufacturing defects or excessive material inconsistencies not present within the vast majority of the other resistors. Gould's subtractive embedded resistors exhibit a positive shift in resistance with a most frequently occurring, peak interval of approximately 2.4% while MacDermid's additive resistors reveal a negative shift with a most frequently occurring, peak interval of approximately -1.92%. Gould's manufacturing process demonstrates slightly more variance, $\sigma = 6.54$, while MacDermid is tighter, $\sigma = 1.27$.

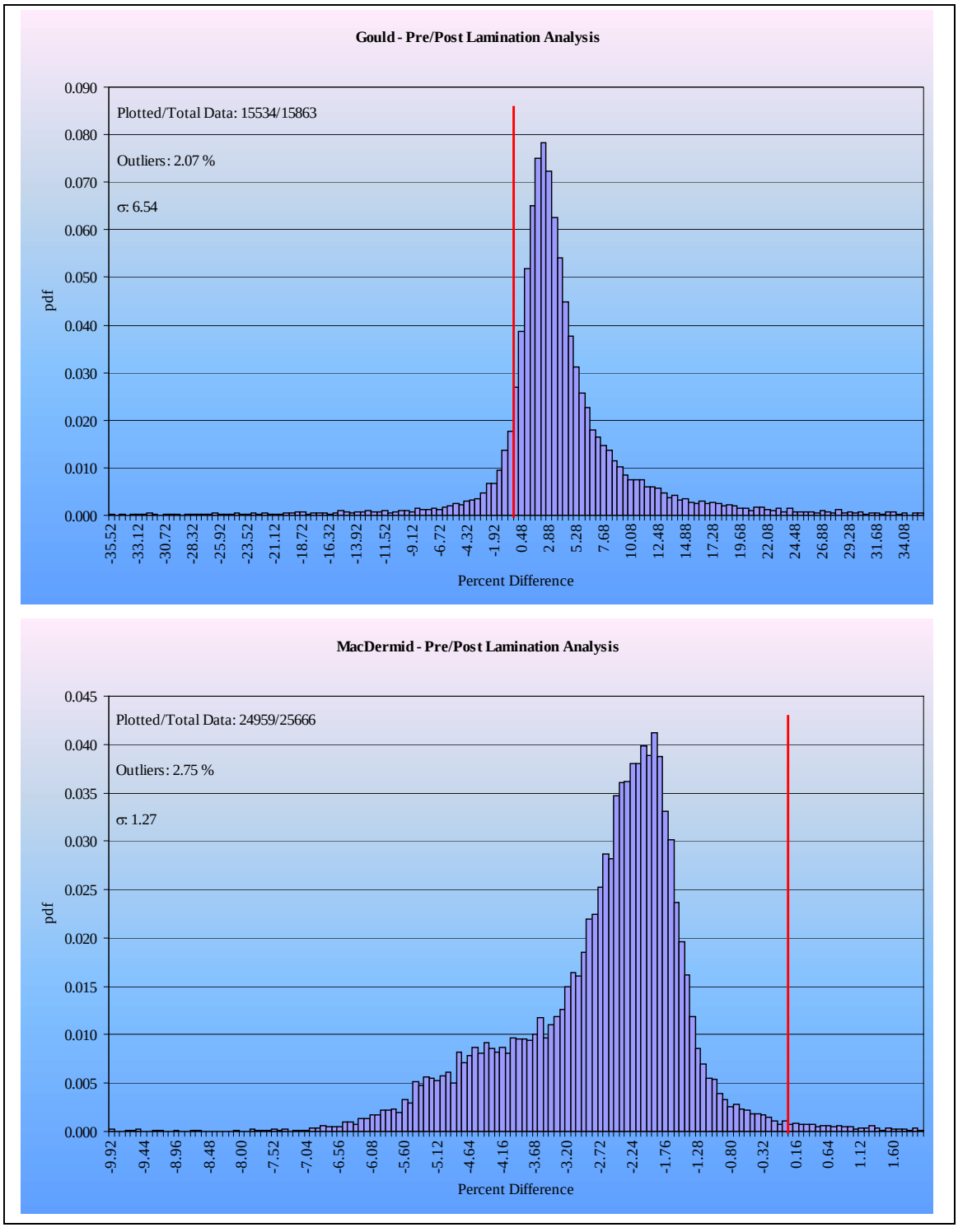


Figure 3.3: Pre/Post lamination analysis

3.3 THERMAL CHARACTERISTICS

To determine the temperature coefficient of resistance (TCR) for both embedded resistor technologies, test samples were subjected to a linearly increasing temperature profile ranging from -25^{o}C to 125^{o}C ramped over a 4 hour time period. Gould embedded resistors exhibited a positively weighted distribution for TCR while MacDermid embedded resistors revealed an even distribution between negative and positive TCR. However, the Gould TCR is an order of magnitude greater than MacDermid's which had a negligible response to the temperature profile. Approximately, 92% of Gould's resistors fell within the peak interval of the distribution (TCR=205.2 ppm/^{o}C) while 12.4% of MacDermid's fell into its peak interval (TCR=-13.89 ppm/^{o}C). Figures 3.4 and 3.5 provide time-dependent resistance versus temperature representation for both Gould and MacDermid embedded resistors exhibiting a linear relationship between resistance and temperature. Figures 3.6 through 3.11 illustrate aggregate embedded resistor thermal characteristics for both Gould and MacDermid technologies for all possible measurable quantities as well as present segregations between horizontal and vertical orientations and reworked and non-reworked resistor configurations. Table 3.1 provides a comparison between the most frequently occurring, peak interval of the distribution and standard deviation for both manufacturers' embedded resistor technologies.

Table 3.1: TCR comparison between Gould and MacDermid embedded resistors

	Configuration	Peak Interval (ppm/°C)		Standard Deviation	
Gould	All Data/Magnified Interval	205.02	189.25	37.56	
	Horizontal/Vertical Orientation	205.02	205.02	49.01	22.93
	Reworked/Non-Reworked	205.02	205.02	9.09	51.85
MacDermid	**Configuration**	**Peak Interval (ppm/°C)**		**Standard Deviation**	
	All Data/Magnified Interval	-13.89	-10.00	26.01	
	Horizontal/Vertical Orientation	-2.27	-13.89	26.10	26.00
	Reworked/Non-Reworked	3.54	-8.08	25.24	25.43

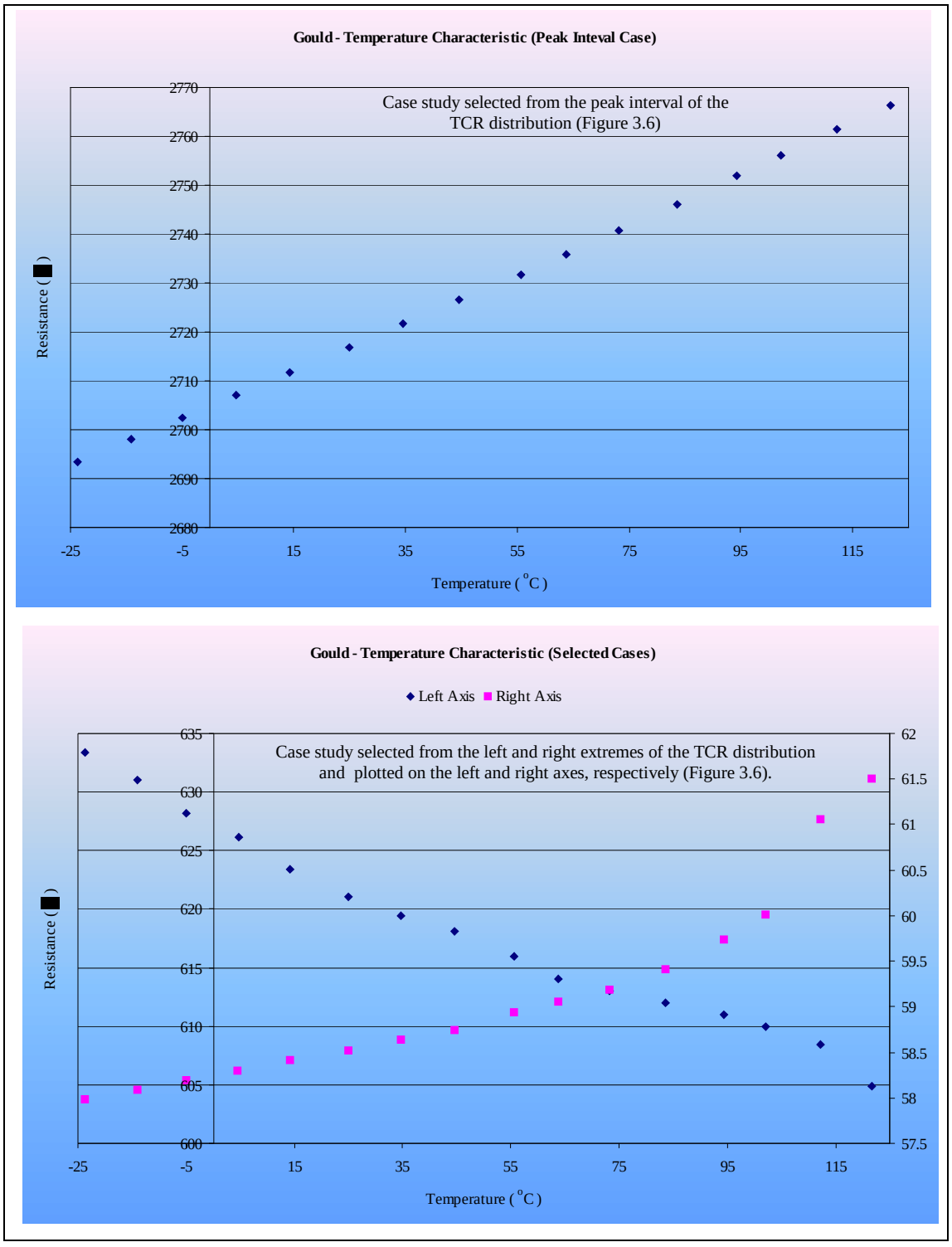


Figure 3.4: Resistance versus temperature representation for Gould embedded resistors

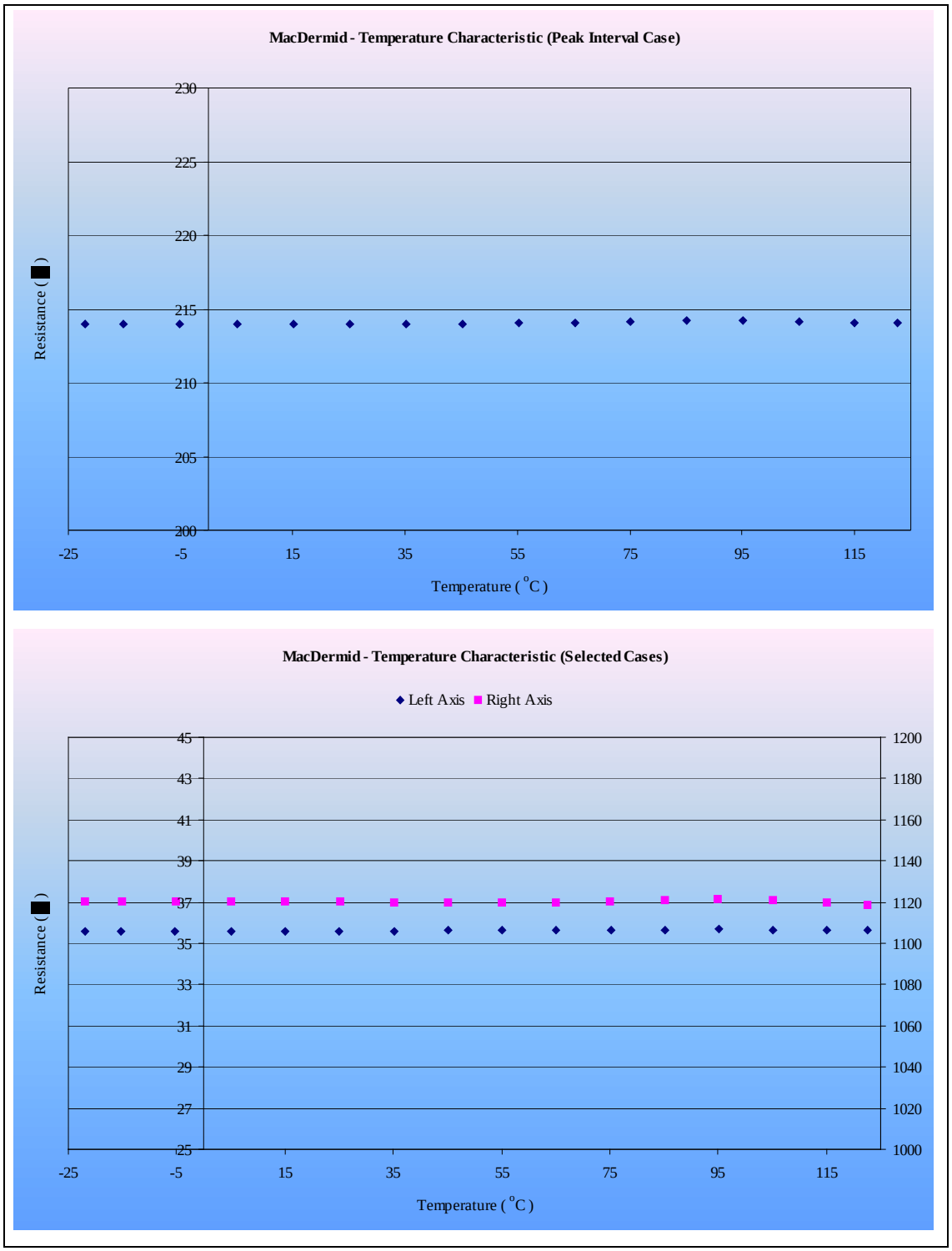


Figure 3.5: Time-dependent resistance versus temperature representation for MacDermid embedded resistors

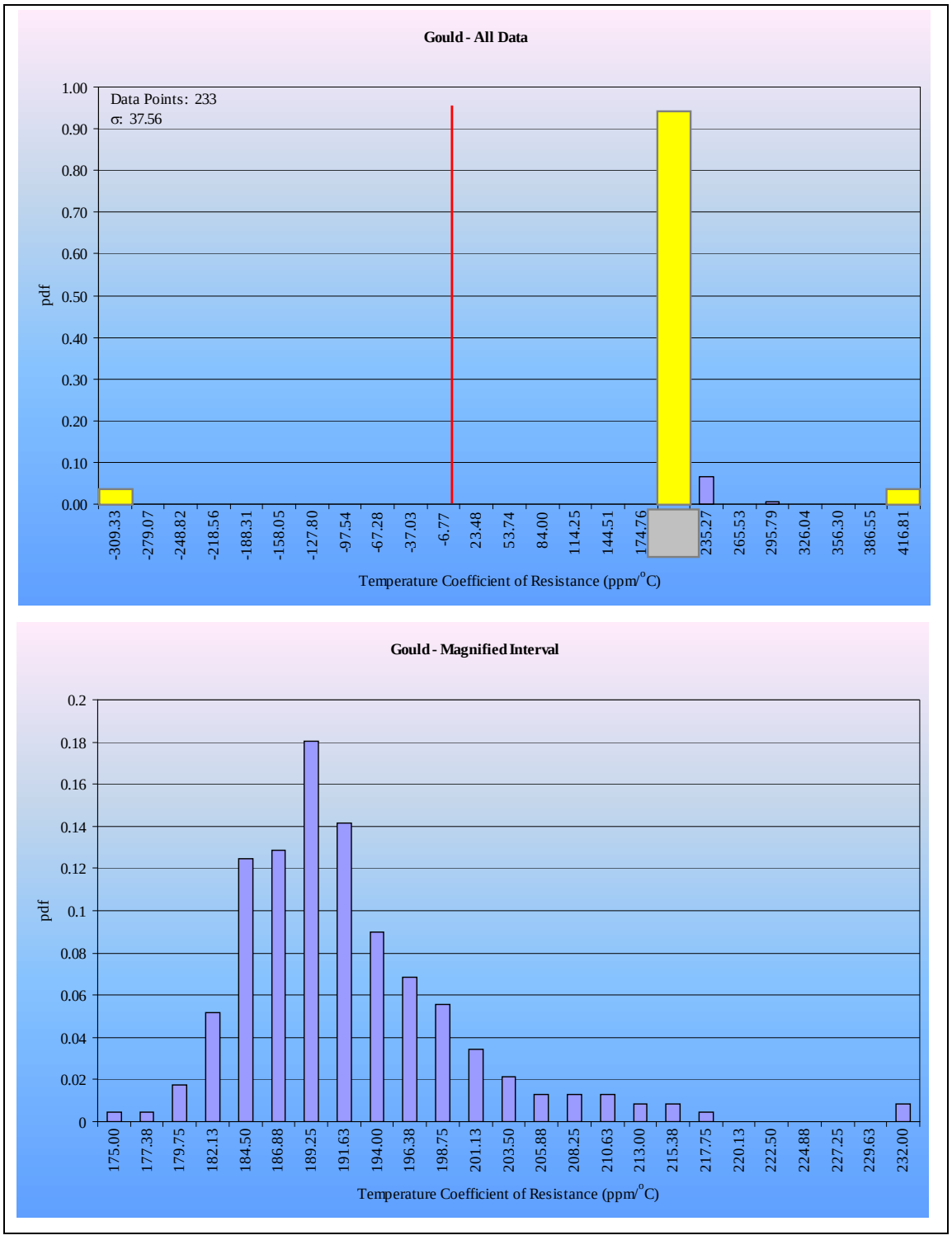


Figure 3.6: Gould embedded resistor TCR

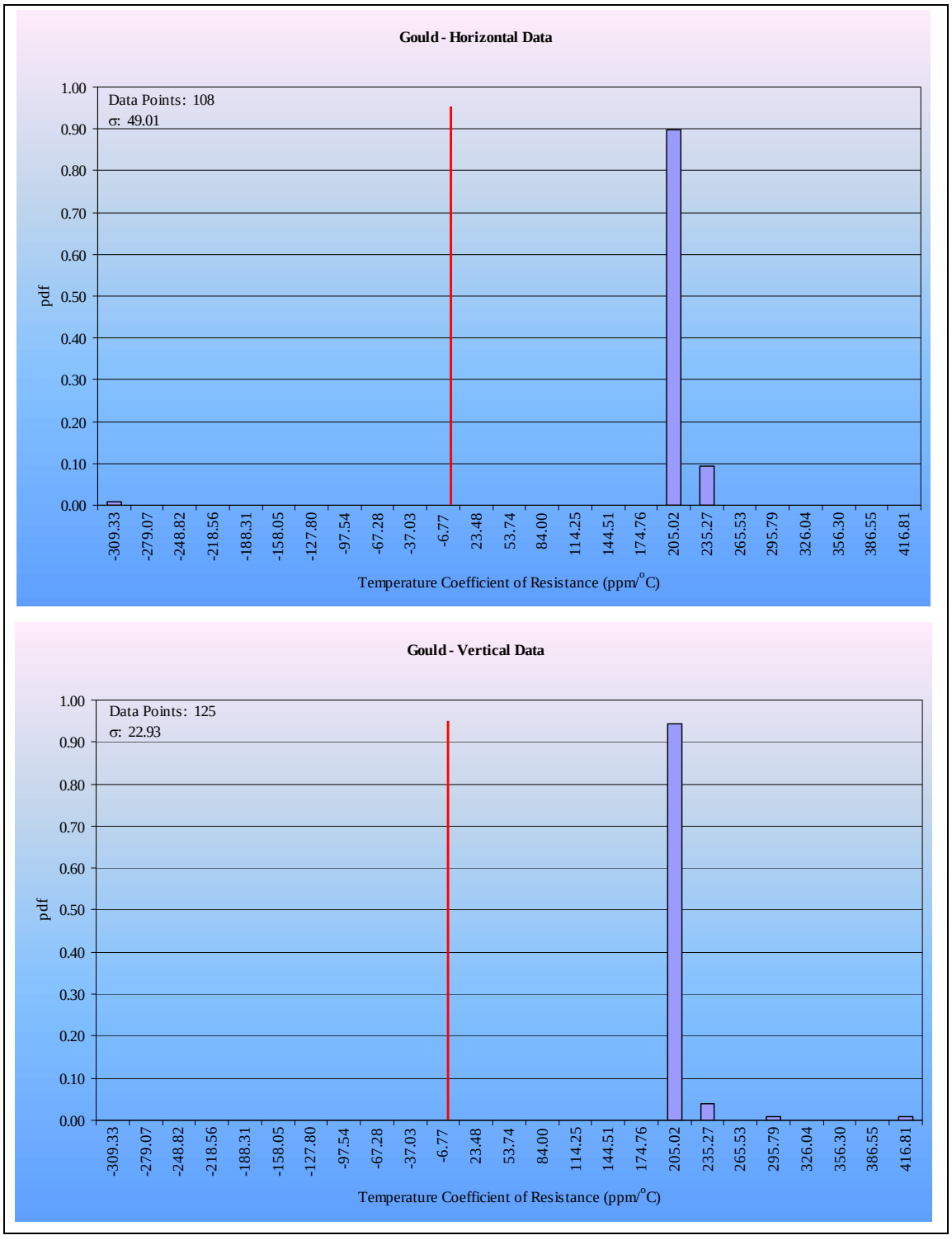


Figure 3.7: Gould embedded resistor TCR sorted by orientation

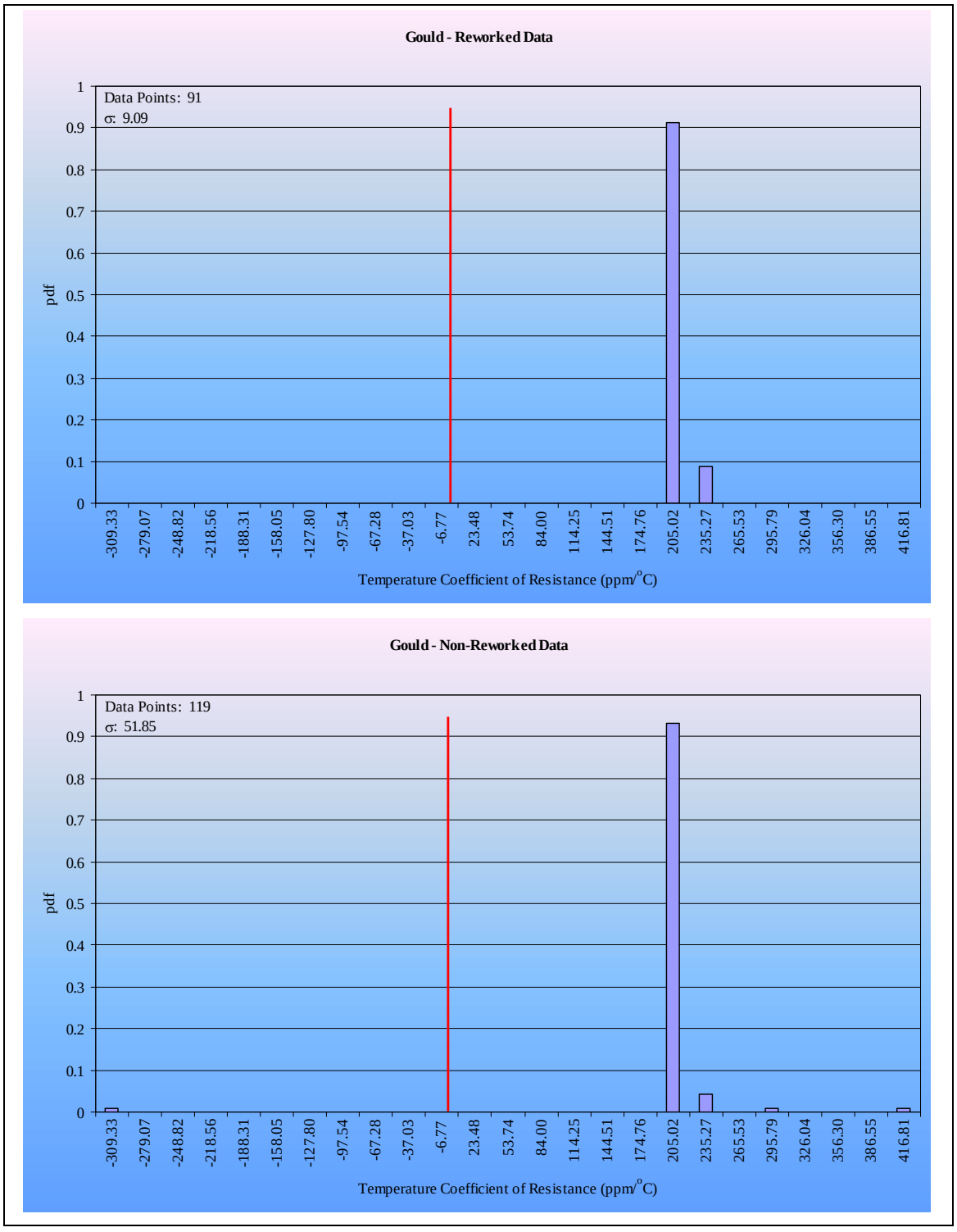


Figure 3.8: Gould embedded resistor TCR sorted by rework

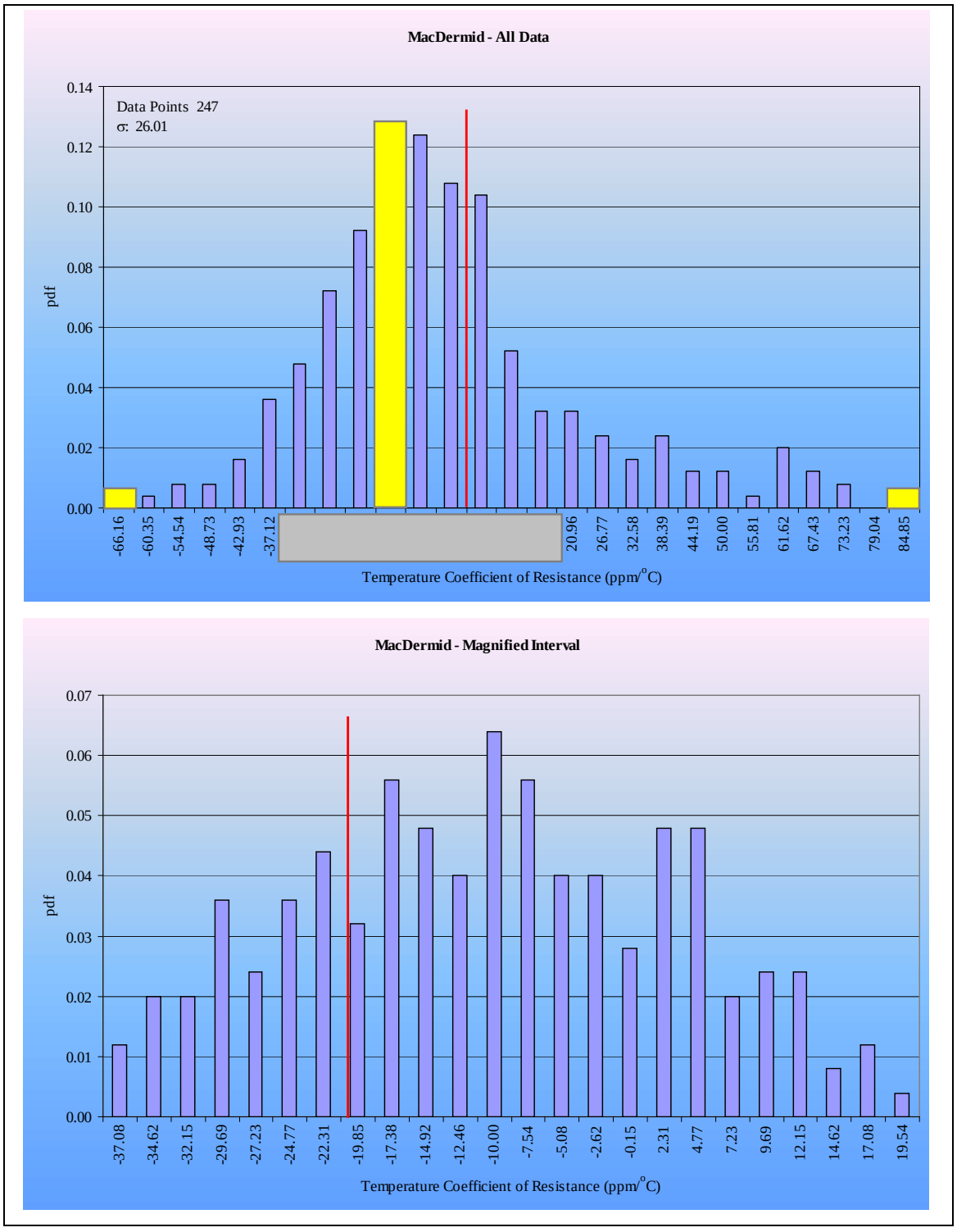


Figure 3.9: MacDermid embedded resistor TCR

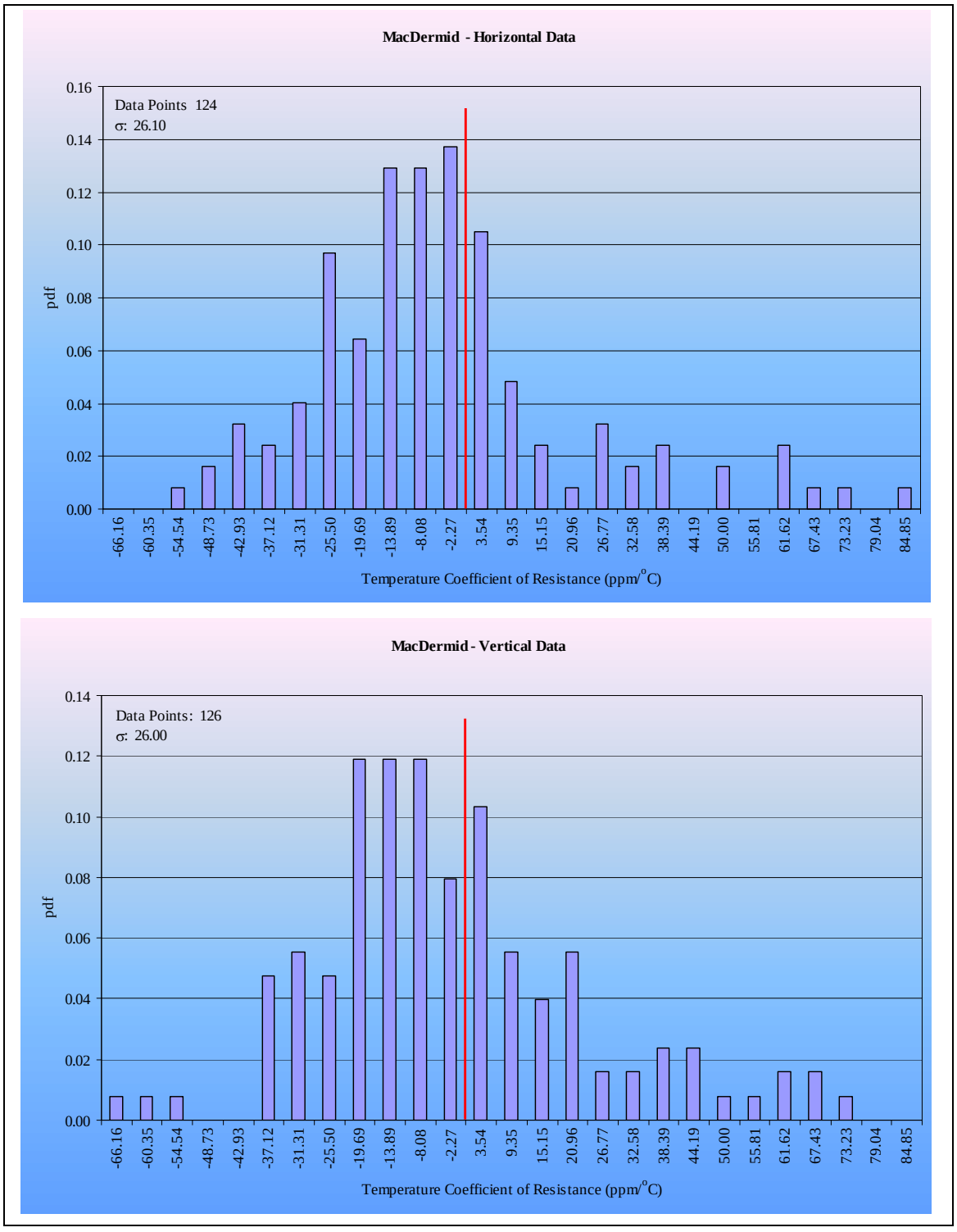


Figure 3.10: MacDermid embedded resistor TCR sorted by orientation

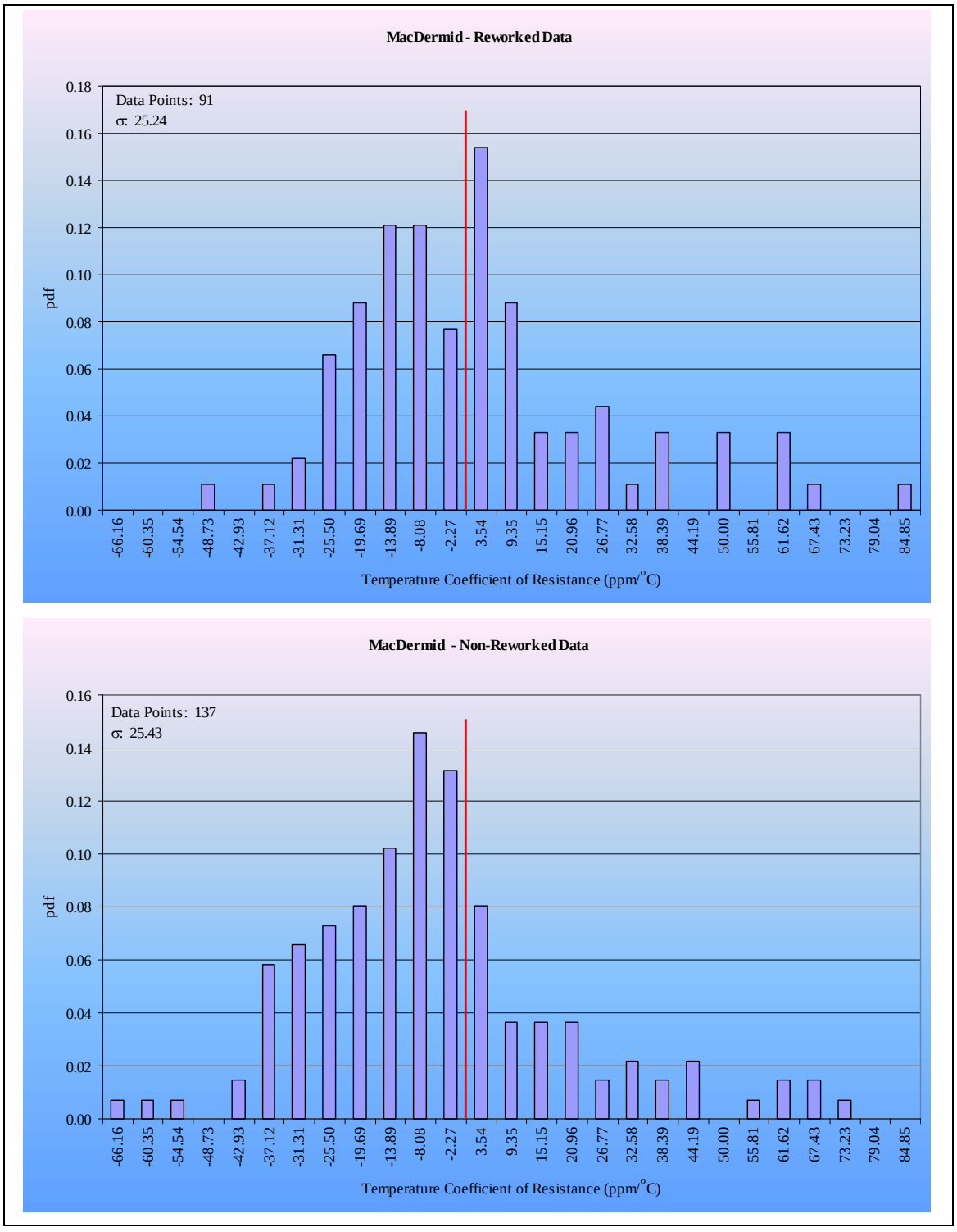


Figure 3.11: MacDermid embedded resistor TCR sorted by rework

3.4 STABILIZATION BAKE ANALYSIS

To determine the sensitivity of the TV-1R test vehicle to storage at elevated temperatures without electrical stress applied, a stabilization bake at 105^{o}C for 2400 hours was performed. Gould embedded resistors exhibited a symmetric distribution of resistance change while MacDermid resistors are weighted toward increases in resistance (positively). The peak interval for MacDermid was an order of magnitude greater than Gould's, 2.36% and 0.78%, respectively; however, the entire spread of response for both technologies was about the same. Approximately, 71% of Gould's embedded resistors fell into the peak interval while 56% fell into MacDermid's. Gould's resistors stabilized more quickly than MacDermid's at 750 hours to MacDermid's 1500 hours. MacDermid's embedded resistors have a prolonged stabilization directly resulting from one less annealing procedure than Gould's during the manufacturing process. Figures 3.12 and 3.13 provide percent change versus time for a median case resistor as well as aggregate percent change after 2400 hours for all embedded resistor measurements. The remainder of the figures providing time-dependent representation and histograms illustrating aggregate embedded resistor response segregated by resistor configuration can be found in Appendix B (Figures B.1 through B.6). Table 3.2 provides a comparison between the most frequently occurring, peak interval of the distribution and standard deviation for both manufacturers' materials/approaches of embedded resistors.

Table 3.2: Stabilization bake comparison after 2400 hours

	Configuration	Peak Interval (Percent Change)		Standard Deviation	
Gould	All Data/Magnified Interval	0.78	0.31	3.81	
	Horizontal/Vertical Orientation	0.78	0.78	4.21	3.47
	Reworked/Non-Reworked	0.78	0.78	3.01	4.38
MacDermid	**Configuration**	**Peak Interval (Percent Change)**		**Standard Deviation**	
	All Data/Magnified Interval	2.36	1.38	3.05	
	Horizontal/Vertical Orientation	2.36	2.36	3.52	2.42
	Reworked/Non-Reworked	2.36	2.36	4.29	1.12

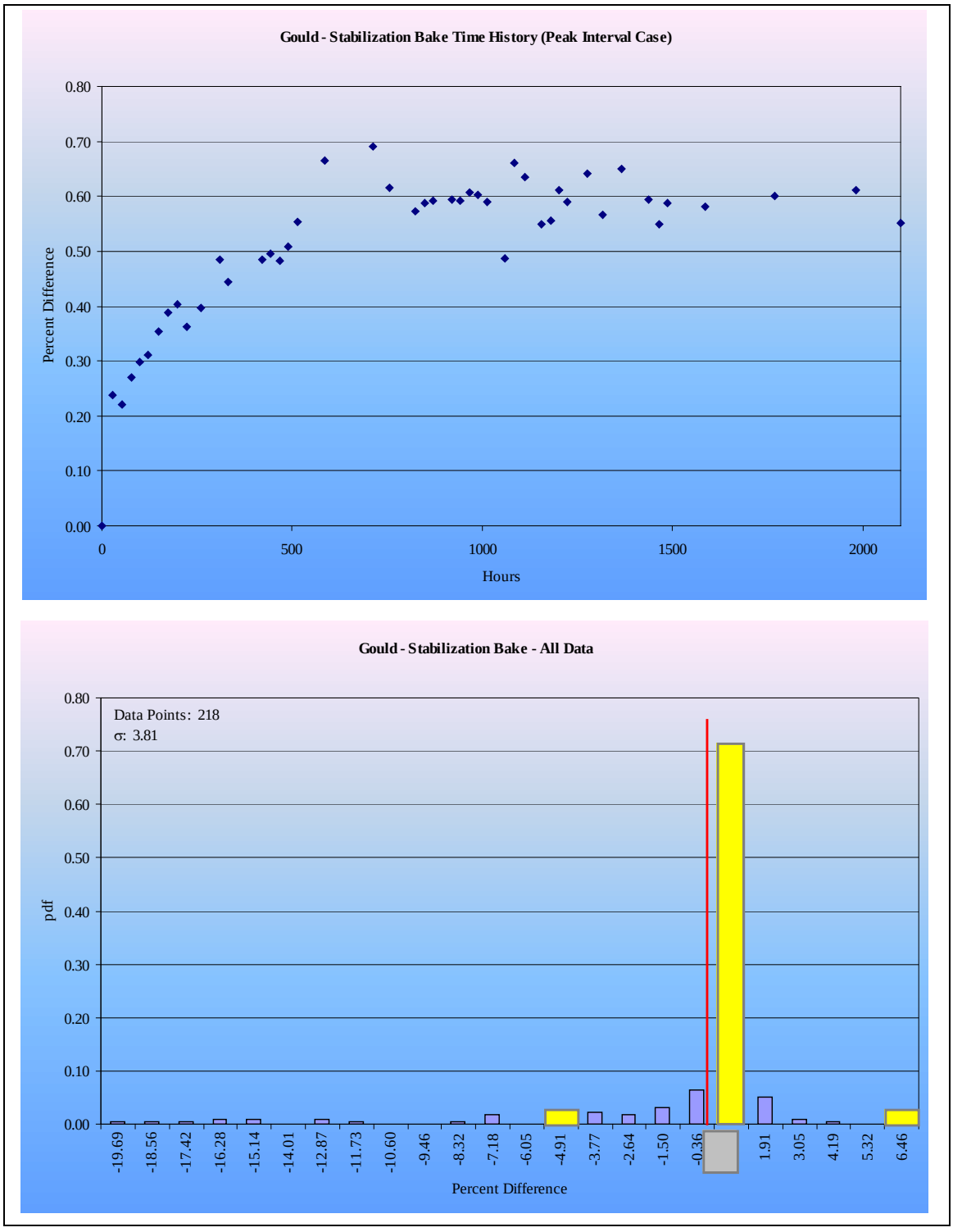


Figure 3.12: Gould embedded resistor stabilization bake analysis after 2400 hours

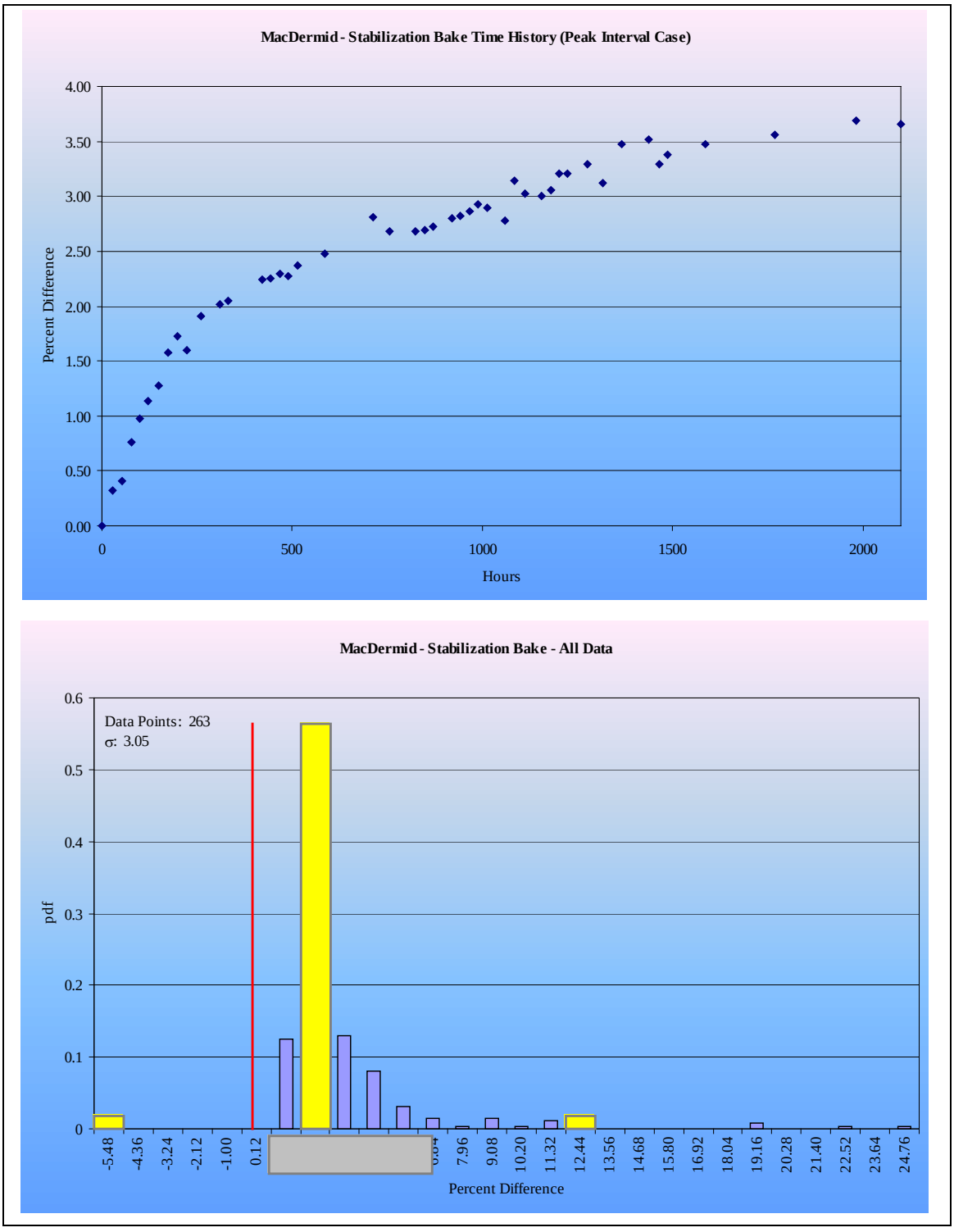


Figure 3.13: MacDermid embedded resistor stabilization bake analysis after 2400 hours

3.5 TEMPERATURE CYCLING ANALYSIS

To determine the sensitivity of the TV-1R test vehicle to extremes of high and low temperatures and the effect of alternate exposures to those extremes, temperature cycling between -65^{o}C and 125^{o}C for 500 cycles was performed. Gould embedded resistors exhibited a symmetric distribution between negative and positive response to the temperature cycling profile while MacDermid resistors were weighted toward increases in resistance (positively). Approximately, 76% of the data fell into the peak interval of the distribution for Gould's resistors, while 87% of MacDermid's resistors fell into its peak interval. However, both manufactures technologies responded with an approximate, most frequently occurring 1% change after 500 cycles. In addition, Gould's embedded resistors stabilized immediately after 20 cycles meanwhile MacDermid's took almost 450 cycles. Figures 3.14 and 3.15 provide percent change versus cycles for a median case resistor as well as aggregate percent change after 500 cycles for all embedded resistor measurements. The remainder of the figures illustrating aggregate embedded resistor response segregated by resistor configuration can be found in Appendix B (Figures B.7 through B.12). Table 3.3 provides a comparison between the most frequently occurring, peak interval of the distribution and standard deviation for both manufacturers' materials/approaches of embedded resistors.

Table 3.3: Temperature cycling comparison after 500 cycles

	Configuration	Peak Interval (Percent Change)		Standard Deviation	
Gould	All Data/Magnified Interval	0.91	-0.10	4.40	
	Horizontal/Vertical Orientation	0.91	0.91	4.37	4.45
	Reworked/Non-Reworked	0.91	0.91	2.58	5.67
MacDermid	**Configuration**	**Peak Interval (Percent Change)**		**Standard Deviation**	
	All Data/Magnified Interval	1.58	0.69	2.96	
	Horizontal/Vertical Orientation	1.58	1.58	1.71	3.85
	Reworked/Non-Reworked	1.58	1.58	2.51	3.25

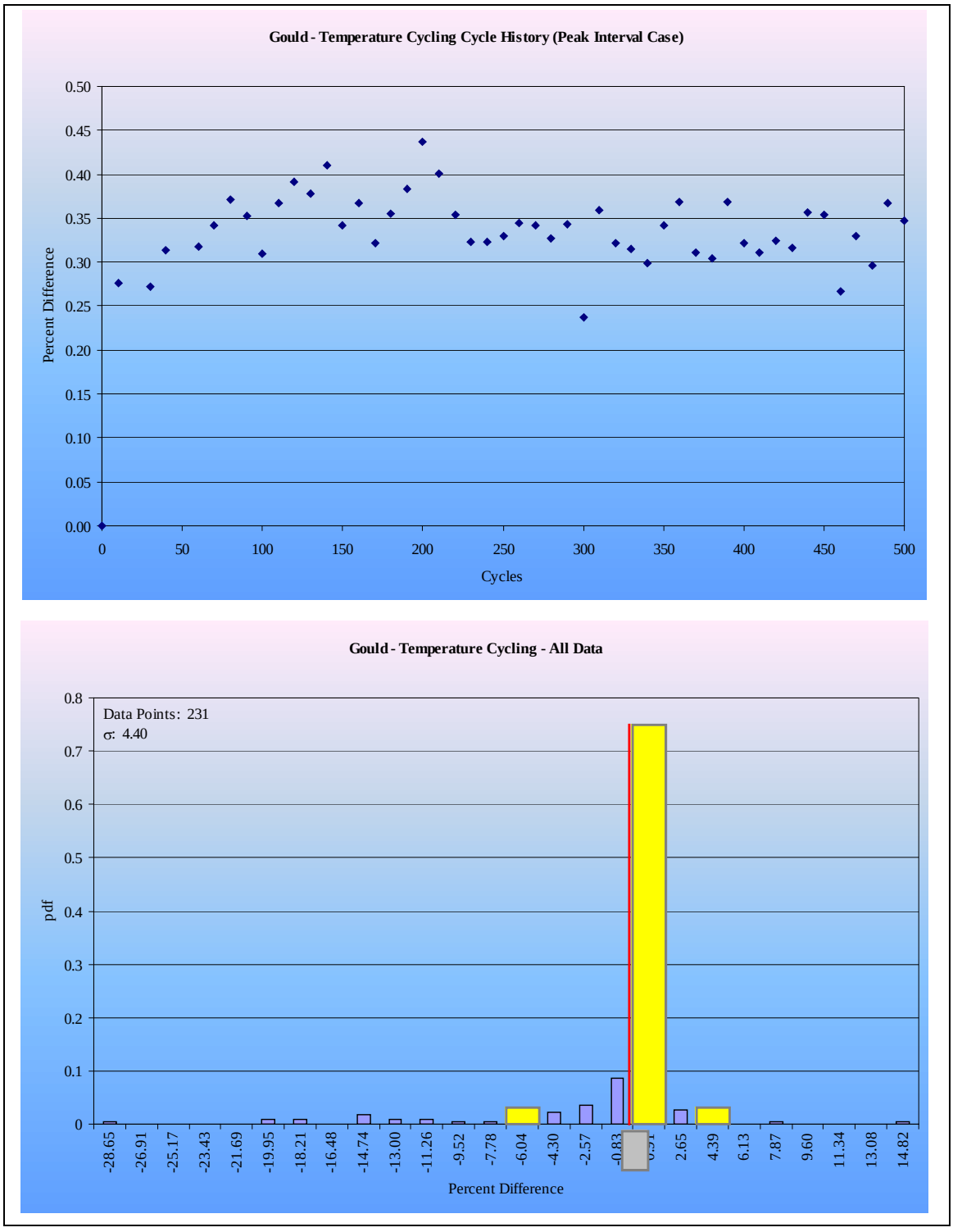


Figure 3.14: Gould embedded resistor temperature cycling analysis after 500 cycles

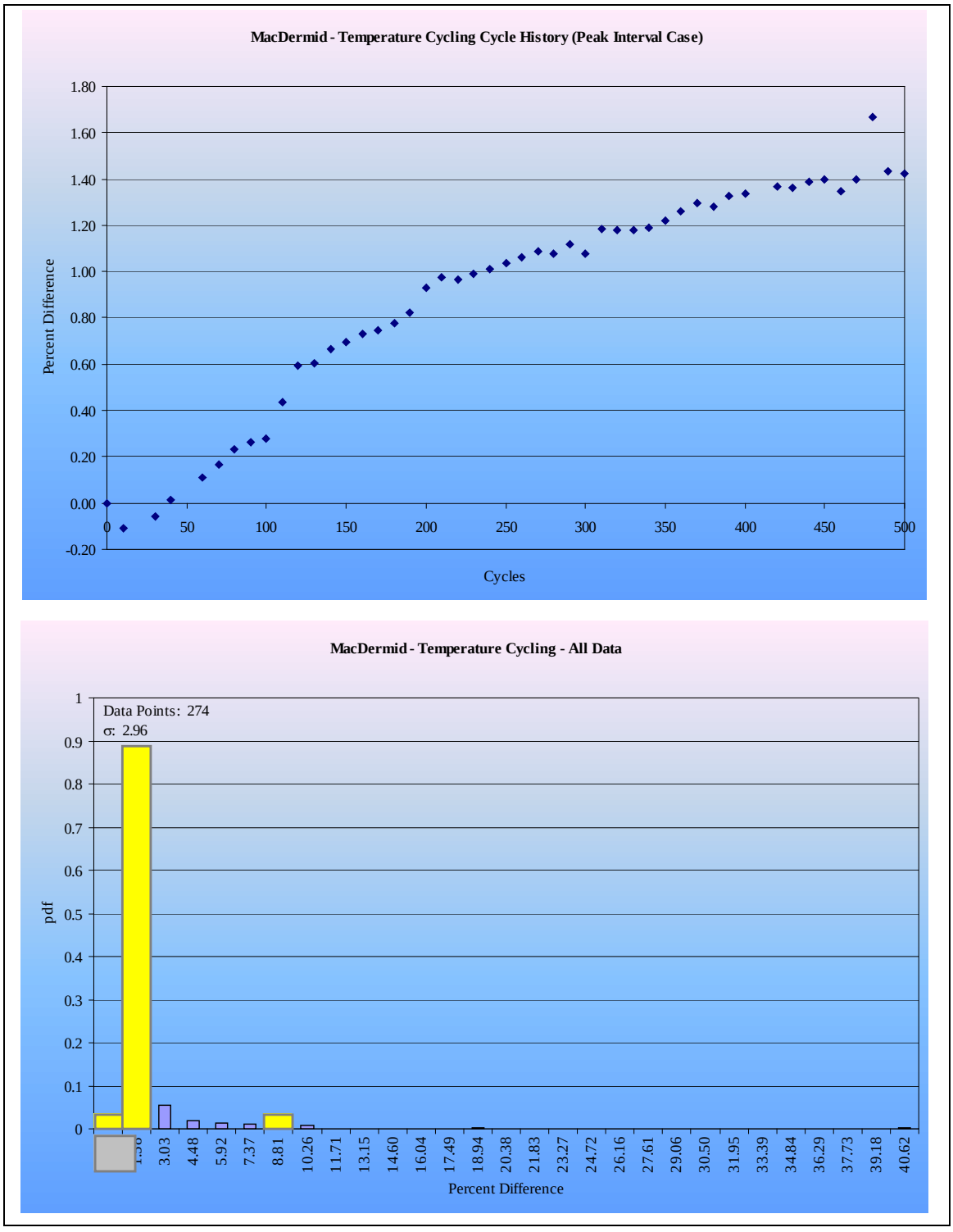


Figure 3.15: MacDermid embedded resistor temperature cycling analysis after 500 cycles

3.6 THERMAL SHOCK ANALYSIS

To determine the sensitivity of the TV-1R test vehicle to sudden exposure to extreme changes in temperature and the effect of alternate exposure to those extremes, thermal shocking between -40^{o}C and 120^{o}C for 500 cycles was performed. Gould embedded resistors exhibited a negatively weighted distribution with a positive peak interval while MacDermid resistors were weighted positively except for a few measurements falling into the negative region. After 500 cycles, approximately 50% of the data fell into the peak interval of the distribution for Gould's resistors (1.68%), while 81% of MacDermid's resistors fell into its peak interval (2.76%). In addition, neither technology stabilized after the subsequent 500 cycles. Figures 3.16 and 3.17 provide percent change versus cycles for a median case resistor as well as aggregate percent change after 500 cycles for all embedded resistor measurements. The remainder of the figures illustrating aggregate embedded resistor response segregated by resistor configuration can be found in Appendix B (Figures B.13 through B.18). Table 3.4 provides a comparison between the most frequently occurring, peak interval of the distribution and standard deviation for both manufacturers' materials/approaches of embedded resistors.

Table 3.4: Thermal shock comparison after 500 cycles

	Configuration	Peak Interval (Percent Change)		Standard Deviation	
Gould	All Data/Magnified Interval	1.68	0.26	4.36	
	Horizontal/Vertical Orientation	1.68	1.68	4.85	3.88
	Reworked/Non-Reworked	1.68	1.68	3.61	4.96
MacDermid	**Configuration**	**Peak Interval (Percent Change)**		**Standard Deviation**	
	All Data/Magnified Interval	2.76	0.98	3.71	
	Horizontal/Vertical Orientation	2.76	2.76	5.25	0.29
	Reworked/Non-Reworked	2.76	2.76	5.62	0.30

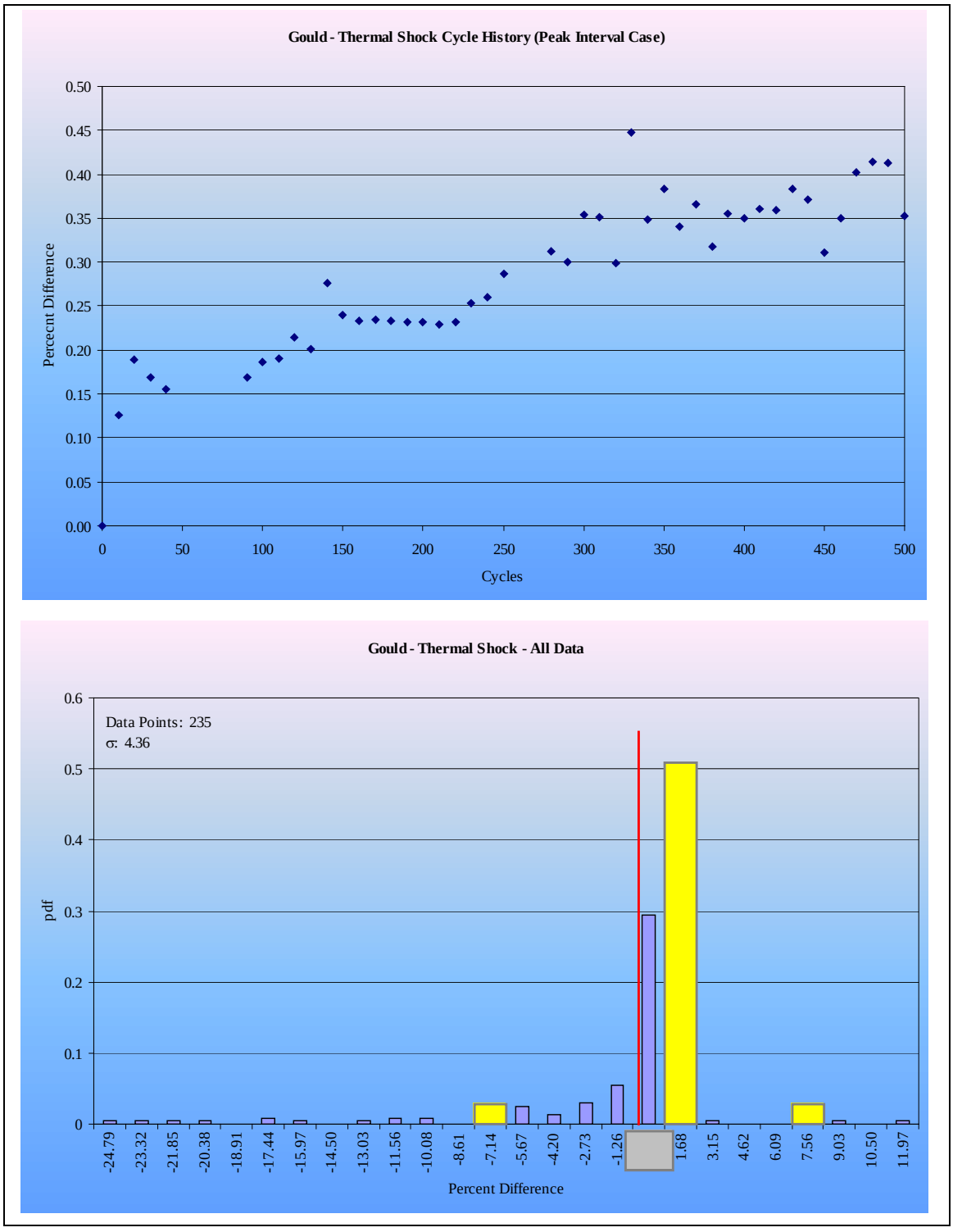


Figure 3.16: Gould embedded resistor thermal shock analysis after 500 cycles

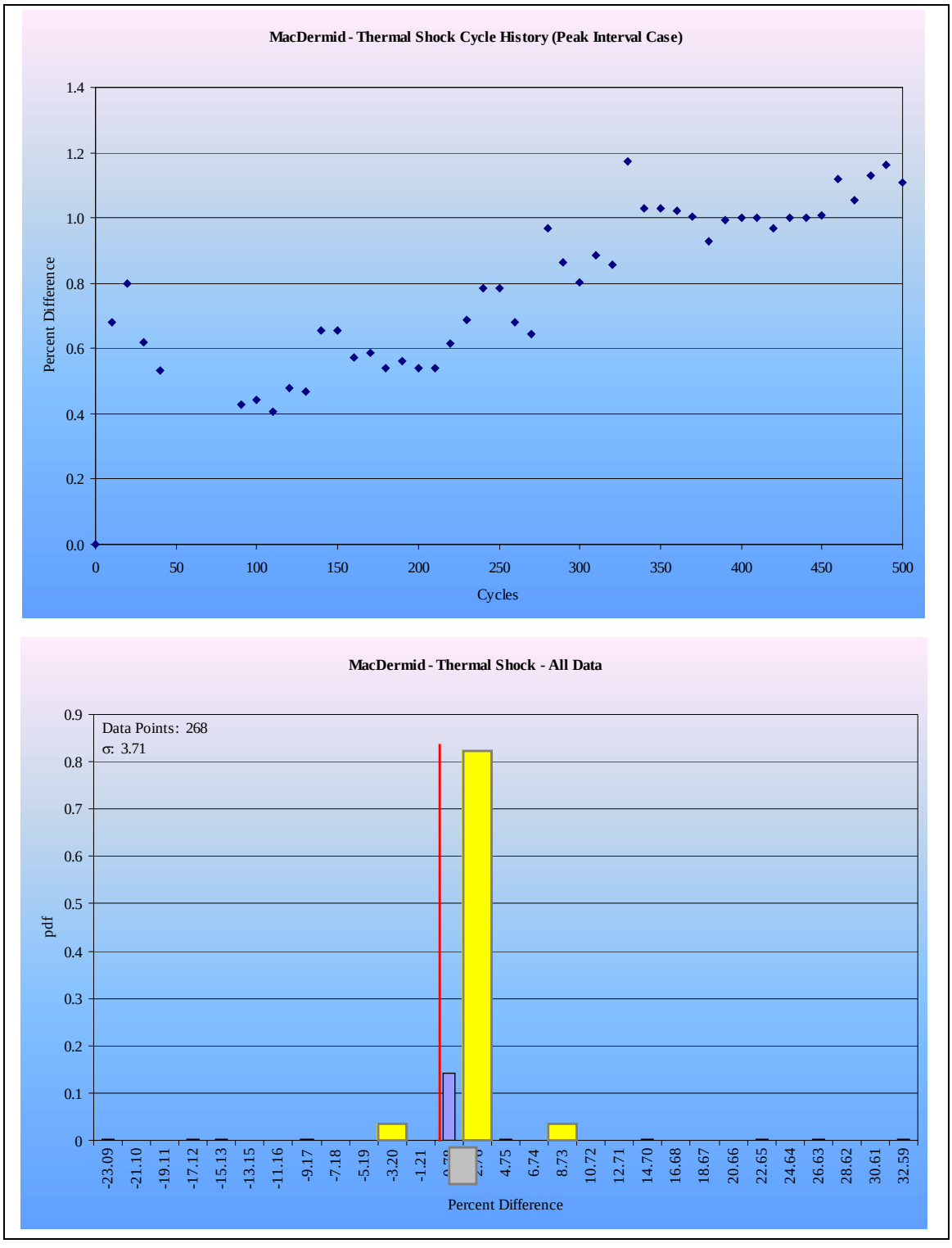


Figure 3.17: MacDermid embedded resistor thermal shock analysis after 500 cycles

3.7 TEMPERATURE/HUMIDITY ANALYSIS

To determine the reliability characteristics of the TV-1R test vehicle to humid environments, temperature/humidity accelerated aging was performed at 130^{o}C with 85% relative humidity under 2.325atm. Both Gould and MacDermid embedded resistors exhibited positively weighted distributions with a few measurements falling into the negative region. After 1244 hours, approximately 39% of the data fell into the peak interval of the distribution for Gould's resistors (6.74%), while only 9% fell into MacDermid's peak interval (27.77%). In addition, Gould's resistor technology stabilized after 800 hours meanwhile MacDermid's resistors took approximately 900 hours. Figures 3.18 and 3.19 provide percent change versus time for a median case resistor as well as aggregate percent change after 1244 hours for all embedded resistor measurements. The remainder of the figures illustrating aggregate embedded resistor response segregated by resistor configuration can be found in Appendix B (Figures B.19 through B.24). Table 3.5 provides a comparison between the most frequently occurring, peak interval of the distribution and standard deviation for both manufacturers' technologies of embedded resistors.

Table 3.5: Temperature/humidity comparison after 1244 hours

	Configuration	Peak Interval (Percent Change)		Standard Deviation	
Gould	All Data/Magnified Interval	6.74	8.33	8.80	
	Horizontal/Vertical Orientation	10.64	6.74	8.30	9.21
	Reworked/Non-Reworked	6.74	6.74	8.91	8.55
MacDermid	**Configuration**	**Peak Interval (Percent Change)**		**Standard Deviation**	
	All Data/Magnified Interval	27.77	22.75	13.56	
	Horizontal/Vertical Orientation	27.77/30.46	27.77/30.46	12.34	14.58
	Reworked/Non-Reworked	22.39	27.77	13.80	13.38

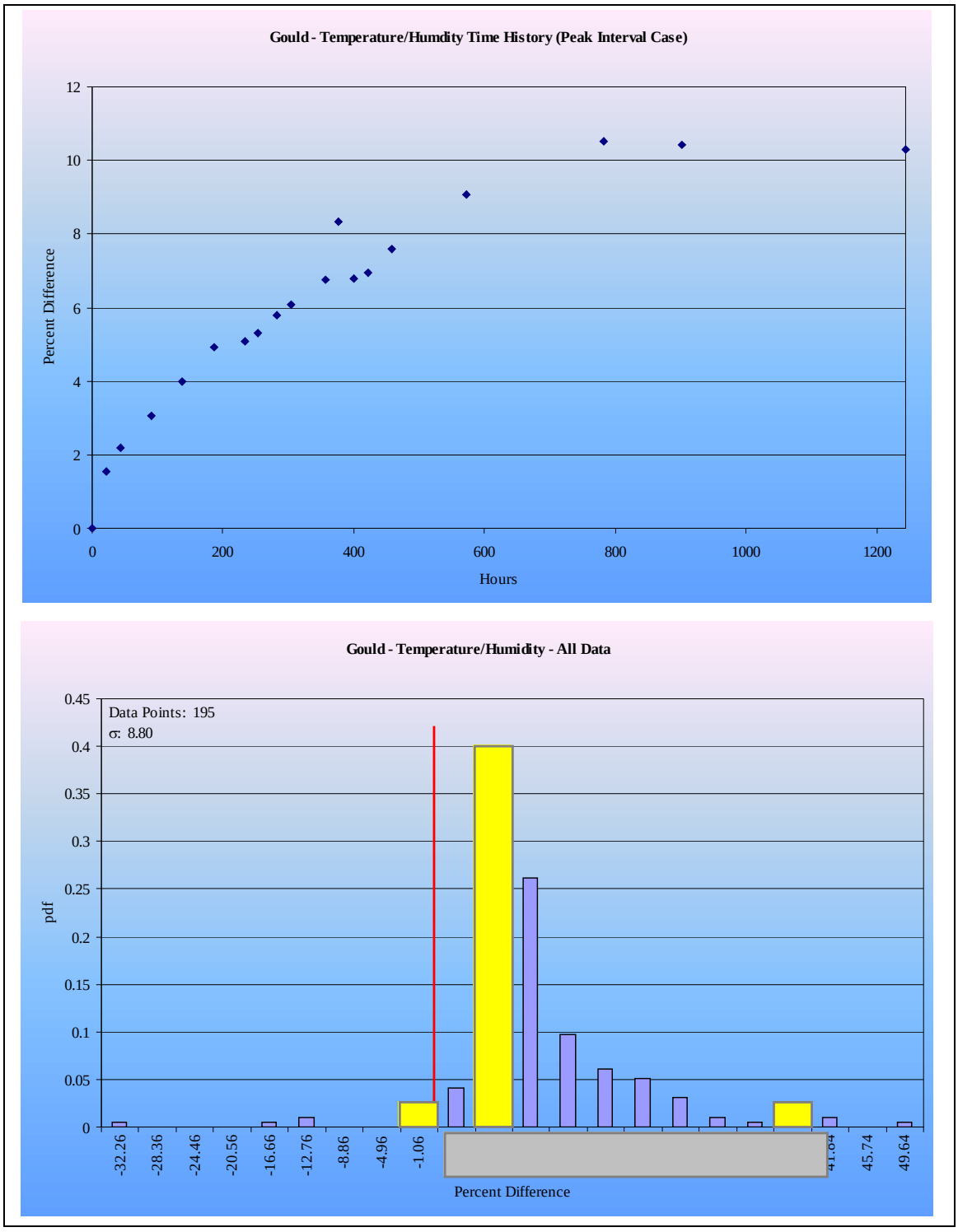


Figure 3.18: Gould embedded resistor temperature/humidity analysis after 1244 hours

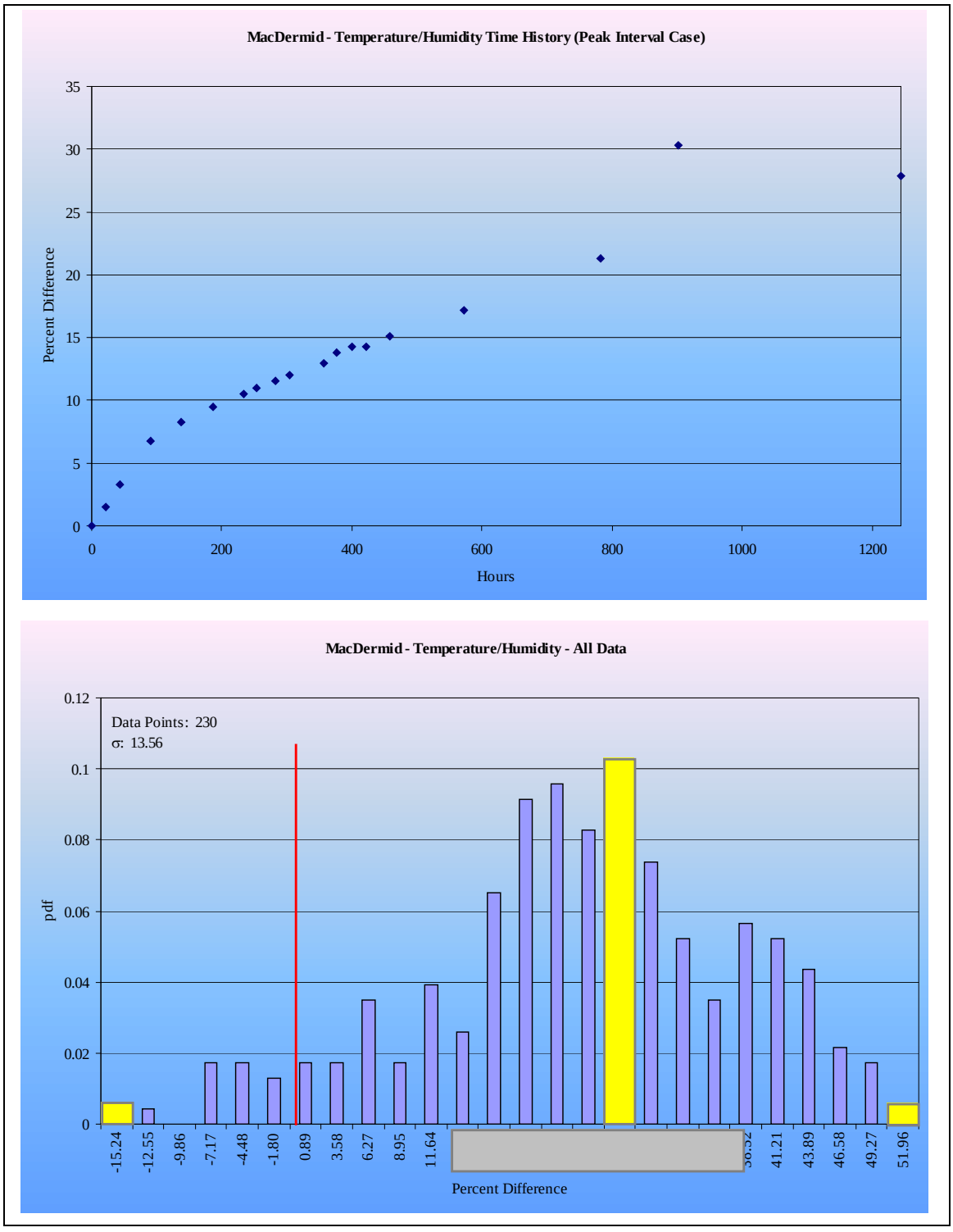


Figure 3.19: MacDermid embedded resistor temperature/humidity analysis after 1244 hours

3.8 MATERIAL STABILITY ASSESSMENT

The stability of a resistor refers to how its resistance changes with time under stressed conditions, e.g., temperature. These changes may be due to recrystallization, hydration, oxidation, and/or other chemical alterations of the resistor material as well as effects at the conductor-resistor interface [Ulrich *et al.*2003]. Traditional resistor technologies are classified according to several parameters depending on the specific needs of electronic system manufacturers including: ohmic value, tolerance, stability during storage or operation, and dissipation [Zandman *et al.*2001]. Table 3.6 provides an overview of several resistor technologies as a function of the required precision.

Table 3.6: Breakdown of established resistor types as a function of precision [Zandman *et al.*2001]

Class	Resistive Element	Tolerance %	Stability %	Maximum TCR (ppm/^{o}C)
High precision	Wirewound Metal foil Thin film	0.005, 0.01, 0.025, 0.05, 0.1	0.05, 0.1	± 5, ± 10
Precision	Wirewound Metal film	0.1, 0.25, 0.5	0.25, 0.5	± 10, ± 25
Semi precision	Wirewound Metal film Metal oxide film Pyrolytic carbon film Cermet	1, 2, 5	1, 2, 5	+200 ± 50, ± 100, ± 100, -500
Standard	Wirewound Pyrolytic carbon film	5, 10, 20	5, 10, 20	+200, ± 100, -500

After performing an extensive environmental qualification regimen to the TV-1R test specimens, Gould and MacDermid embedded resistor technologies performance characteristics fit within the semi precision classification for traditional resistor

technologies. Yet, for high speed electronic systems, resistor tolerance is not nearly as important as the elimination of the inductive reactance of surface mount chip components, vias and traces. For these types of resistors, actual tolerance is a combination of the initial mismatch of the device value and line impedance, the device tolerance, and the series inductance and inductive reactance of the device. In a recent *Sequent Computer* study, embedded resistors were found to eliminate almost all of the inductance, and thus reactance, normally associated with discrete resistors and their vias, therefore enabling a 10-15% embedded resistor to exhibit significant signal integrity improvements over chip and discrete resistors of a 1-2% tolerance [Doeling 1998]. Table 3.7 provides a breakdown of both Gould and MacDermid embedded resistor technologies and compares them against Ohmega Technologies' well-established Ohmega-Ply® 50 Ω/square planar resistor technology.

Table 3.7: Breakdown of embedded resistor technologies

Embedded Resistor Manufacturer	Resistive Element	Tolerance %	Stability %	Maximum TCR (ppm/^{o}C)
Gould (50 Ω/square)	Subtractive Nickel Chromium on Copper	1	0.78*	+200
MacDermid (50 Ω/square)	Additive Plated Nickel Phosphorous	1	2.36*	± 80
Ohmega Technologies (50 Ω/square)	Subtractive Nickel Phosphorous on Copper	5	0.75**	- 60

* After 2400 hours at 125^{o}C

** After 1000 hours at 70^{o}C

CHAPTER 4 FAILURE ANALYSIS

4.1 INTRODUCTION

4.1.1 Overview

Failure analysis is a systematic examination of failed devices designed to identify failure sites, modes and mechanisms to determine the root cause and recommend failure prevention methods to improve product reliability [Devaney *et al.*1983]. Failures occur for any number of reasons including: design flaws, poor quality materials, manufacturing problems, improper conditions during transport or storage, overstress during operation, etc. and must be isolated in order to take corrective action. Failure analysis techniques include three hierarchical levels of examination. Level I entails visually inspecting a device with the naked eye and/or an optical microscope to locate possible failure sites. Level II employs non-destructive methods used to hone in on possible failure modes. Finally, Level III applies destructive methods used to pinpoint exact failure mechanisms. Chapter 4 focuses on the hierarchical failure analysis method used to extract the failure mechanisms associated with Gould and MacDermid's embedded resistor technologies used in printed wiring boards.

4.1.2 Failure Definition

Since electronic system specifications generally differ from application to application, defining boundary limits constituting exactly what a failure entails becomes an arduous task as the number applications grow. For one electronic system, resistance tolerances within ± 20% might be acceptable (e.g., digital logic line terminations)

meanwhile for another system, ± 1% difference might be all the system can tolerate (e.g., analog systems). Therefore, this thesis will loosely define a failure as the resulting shift in embedded resistance value greater than ± 50% of the initial unstressed resistor condition or the development of an open or short circuit as consequence of a particular qualification test. Thus after conducting an extensive data analysis regimen, failed embedded resistor cell locations were pinpointed within the TV-1R test vehicle's 20 cell matrix (see Figure 2.2). Table 4.1 provides the amount and configuration of failed resistor measurements for a given experiment.

Table 4.1: Failure Summary*

Qualification Regimen	Embedded Resistor Manufacturer			
	Gould		MacDermid	
Thermal Characteristic (-25°C to 125°C at 0.625°C/min)	Horizontal 0/107	Reworked 0/114	Horizontal 0/129	Reworked 0/113
	Vertical 0/125	Not Reworked 0/118	Vertical 0/127	Not Reworked 0/143
Stabilization Bake (105°C)	Horizontal 1/98	Reworked 1/104	Horizontal 0/136	Reworked 0/115
	Vertical 2/120	Not Reworked 2/114	Vertical 0/128	Not Reworked 0/149
Temperature Cycling (-65°C to 125°C at 5°C/min with 30 min dwell at extremes)	Horizontal 0/113	Reworked 1/119	Horizontal 1/139	Reworked 1/121
	Vertical 2/118	Not Reworked 1/112	Vertical 0/135	Not Reworked 0/153
Thermal Shock (-40°C to 120°C with 5 min dwell)	Horizontal 1/111	Reworked 1/117	Horizontal 0/134	Reworked 0/117
	Vertical 0/125	Not Reworked 0/119	Vertical 0/119	Not Reworked 0/151
Temperature/Humidity (130°C with 85% RH at 2.235atm)	Horizontal 18/95	Reworked 21/100	Horizontal 16/119	Reworked 11/103
	Vertical 29/100	Not Reworked 26/95	Vertical 13/111	Not Reworked 18/127

**Failures defined as $\Delta R > 50\%$ or the development of an open or short circuit*

Two numbers appear below each embedded resistor configuration. The number to the left of a backslash denotes the quantity of failed embedded resistor measurements while the number to the right signifies the quantity of resistor measurements adhering to the specified tolerance limit. Adding the number of failures within each configuration (horizontal/vertical, reworked/not reworked) equals the total amount of embedded resistor measurements that failed as the result of a particular qualification experiment. For example, a total of 47 Gould embedded resistor configurations failed as a result of the temperature/humidity qualification experiment, 18 horizontally and 29 vertically oriented resistor configurations or 21 reworked and 26 not reworked resistor configurations.

4.1.3 Level I: Optical Inspection

After determining cell locations containing failed embedded resistors, each TV-1R board was visually inspected for inconsistencies, generally discolorations within embedded resistors, noticeable to the naked eye (e.g., Figures 4.4a and 4.6a). In this manner, failed embedded resistors could be pinpointed to allow further examination to be conducted. For any cell location in which no information could be ascertained with the naked eye, an optical microscope with 50x resolution was employed to further investigate the embedded resistor cell. Additional verification was conducted with an ohmmeter measuring resistive value across plated through holes located at each end of an embedded resistor. Then the resistor's value was compared to Merix's post lamination results measured in the same manner to ensure the particular resistor was in fact the cause of the induced failure. In this manner, single embedded resistors within daisy chains of

resistors could be located as the cause of a failure. As a result of Level I failure inspection, every failure site was attributed to a specific embedded resistor.

4.1.4 Level II: Non-Destructive Scanning Acoustic Microscope (SAM)

In order to hone in on possible failure modes characteristic of Gould and MacDermid embedded resistor technologies, a scanning acoustic microscope (SAM) was used for Level II non-destructive failure inspection. A SAM utilizes high-frequency ultrasound waves to penetrate surfaces and generate acoustic impedances to produce high resolution images of a sample's interior structure to detect hidden defects, such as interfacial separation, delamination and/or voiding within a device. Due to the nature of ultrasonic waves, samples must be submerged in a liquid or solid medium in order for the high-frequency ultrasound to freely propagate. Once the samples are submerged, the SAM has the ability to operate in two different modes, pulse-echo and through transmission. Pulse-echo operates on the principle that sound reflects whenever a sudden change in density occurs, generally at material interfaces. Under pulse-echo or reflection mode, a transducer emits an ultrasonic signal to a sample and records sound reflections off the sample using the same transducer as a collector. The amount of density change determines the quantity and polarity of the sound reflected. The greater the change, the stronger the return signal. Whatever sound does not reflect back travels through the part to the next interface encountered. Consequently, the intensity, polarity and time that it takes the sound to return to the transducer are stored within a computer that then performs mathematical operations to obtain depth specific information to regenerate an image of the sample's interior structure. Material inconstancies appear as white splotches

in the generated image. Meanwhile, under through transmission, also known as thru mode, through scan or T-scan, a transducer emits an ultrasonic signal into a sample where the sound passes through and then is detected by another transducer placed below the sample. The data obtained is then transposed onto a single imaging plane representing the entire thickness of the sample therefore eliminating the possibility of obtaining depth-specific information. Through scan operates on the principle that if a defect is encountered at any depth within a part, the ultrasound is reflected and no signal is obtained at the receiver. Accordingly, the intensity and time it takes the sound to reach the receiver is stored within a computer. Since material inconstancies reflect the ultrasonic pulses, no sound is received at the collector thus creating a corresponding black splotch within the generated computer image. Meanwhile the rest of the sample's material is illustrated using gray hues. Since through transmission is depth insensitive, it is generally used to validate information obtained under pulse-echo mode. In addition to the two inspection modes, the SAM allows for three types of data collecting scans: A-scan, a representation of the sample when Cartesian coordinate x and y movements are held constant and z-axis (depth) information is rendered as an oscilloscope waveform, B-scan, where a x-z or y-z planar slice of the sample is represented as a 2-dimensional image or C-scan, a representation of the sample when the z-axis is held constant and a x-y planar image is developed. Figure 4.1 illustrates the three types of scans along with examples.

SAM imaging was conducted using a 15MHz transducer to optimize a characteristic resolution/attenuation tradeoff manifested in multilayer PWB samples. The TV-1R boards were submerged in a distilled water medium during testing to allow for

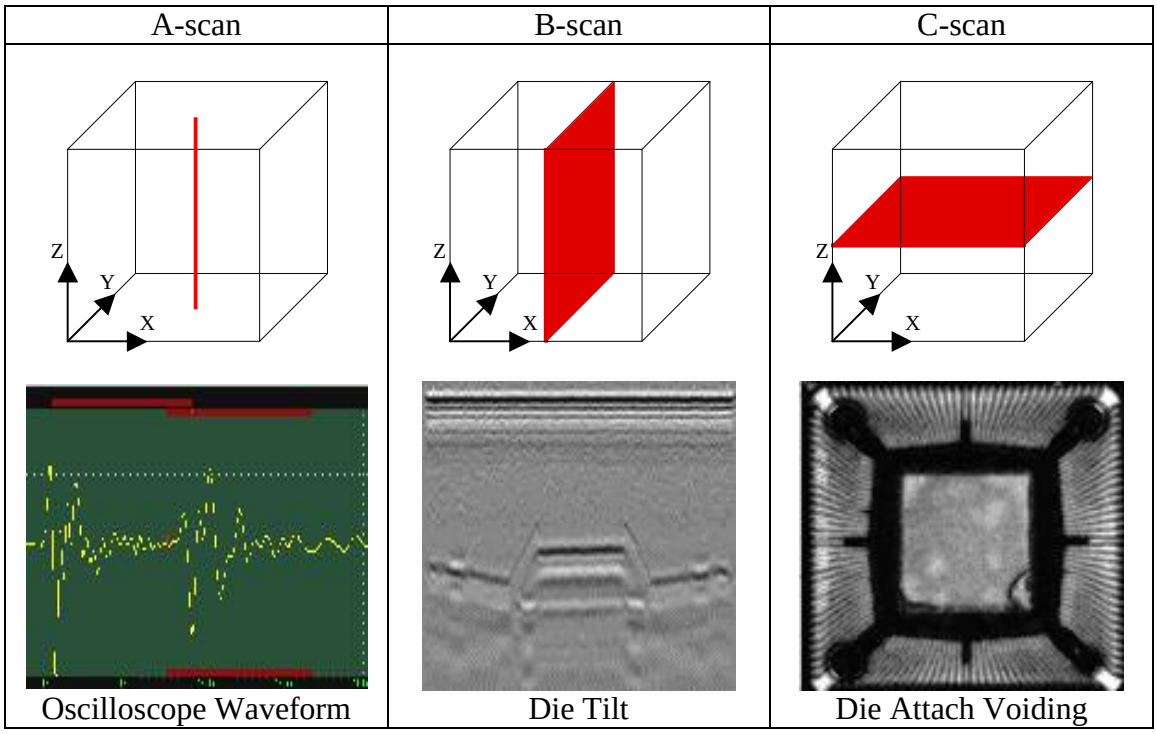


Figure 4.1: SAM data collection scan types with corresponding examples

proper acoustic wave propagation. Both through transmission and pulse-echo modes were used to determine apparent failure modes. During through transmission scanning, samples underwent a material or bulk scan acquired by setting a data gate on a real-time A-Scan to create boundary limits for appropriate travel time/depth specifying the entire thickness of a sample to undergo a subsequent C-Scan. This technique allows multiple interfaces to be superimposed onto one image describing the entire thickness of the sample. As a result, peak amplitude images were generated where only the strength of the ultrasonic wave was measured in decibels with stronger collected signals creating brighter images. Under pulse-echo mode, samples underwent interfacial scanning where a data gate was set on a real-time A-Scan to create boundary limits for appropriate travel time/depth within the sample's thickness to illustrate the material characteristics of a

particular slice of the sample. Again, peak amplitude images were created however under pulse-echo mode phase inversion imagining was also achieved. With phase inversion imaging only the polarity or phase of a reflected ultrasonic wave is measured as a positive, negative or zero value. If the sound travels from a less dense material into a more dense material, a negative signal is produced; the opposite is true of a produced positive signal. Complex mathematical algorithms can then regenerate the sample slice using gray hues overlaid with red and yellow splotches to illustrate detected inconsistencies within the material. In addition, a front surface follower (FSF) was used during pulse-echo scans into order to stabilize the position of the data gate set within the sample's thickness. A FSF enables the front surface of the sample to be tracked allowing the data gate to move dynamically with the variation of the front surface of the sample. Typically, a FSF is used to minimize distortion effects attributable to warped portions of the sample. Figure 4.2 is a depiction of the SAM used for Level II failure inspection.

Figure 4.2: HS1000 HighSpeedTM Scanning Acoustic Microscope [SONIX]

4.1.5 Level III: Destructive PWB Sectioning

Once Level II non-destructive SAM imaging was completed, failed embedded resistors underwent Level III failure inspection, destructive PWB sectioning. TV-1R embedded resistor cells containing failure sites were completely removed from the corresponding test vehicles using a small electronic powered bandsaw cutting along the silkscreen cell boundary lines outlining individual cells within the entire embedded resistor cell matrix described earlier in Chapter 2. After cutting out cells, each individual failure was visually inspected to determine the best directional cut to section an embedded resistor. Once the appropriate directional cut was determined, the bandsaw was employed to section the remaining PWB cell parallel to failure site within a few millimeters of the embedded resistor in question. Next, sectioned samples were vertically supported within a nonporous plastic cylindrical shell filled with a 2-part (10:1 ratio) epoxy resin and allowed to cure for 24 hours. Afterward, the plastic shell was removed from the hardened epoxy resin and the resulting epoxy cylinder containing the sectioned PWB was slowly sanded by hand towards the failure site using incremental steps in aggressive sandpapers ranging from 450 (rough) to 2400 (polishing) grit silicon sandpaper. During periodic intervals, the sectioned samples were observed under an optical microscope to ensure the prevalence of a failure mode within a resistor. Finally, single micron silica aluminum powder was mixed with water to form a polishing paste used to buff the surface of the failure site on a polishing wheel to a shine. Again samples were inspected under an optical microscope to allow magnified digital images of the sectioned embedded resistors to be taken exhibiting particular failure mechanisms within the resistors.

4.1.6 Environmental Scanning Electron Microscope (ESEM)

Due to the thickness of both Gould and MacDermid embedded resistor technologies, not all failure mechanisms were completely visible under an optical 50x magnification microscope. For embedded resistors containing failures that could not be seen optically, an environmental scanning electron microscope (ESEM) was employed. An ESEM is a special type of scanning electron microscope that works under controlled environmental conditions that do not require a conductive coating on inspection samples. Various environments are available including: air, N_2, Ar, 0_2, etc. The ESEM can operate at electron accelerating voltages ranging from 5kV to 30kV at which image resolution is approximately 5nm. The basic setup of any ESEM is an electron column that generates a beam of electrons; a sample chamber where the beam interacts with the sample and strategically placed electron detectors that monitor electron/sample interactions. In addition, every ESEM is coupled with a computerized viewing system that reconstructs the sample from the electronic signals generated by the detectors and a digital imaging system to record events within the ESEM camber. All sectioned embedded resistor samples viewed within the ESEM were pressurized to 2Torr in an air environment using 25kV electron acceleration and maximum 1400x magnification. Figure 4.3 is a depiction of the ESEM used to view sectioned embedded resistors along with a biological sample image of an ant head taken with an ESEM.

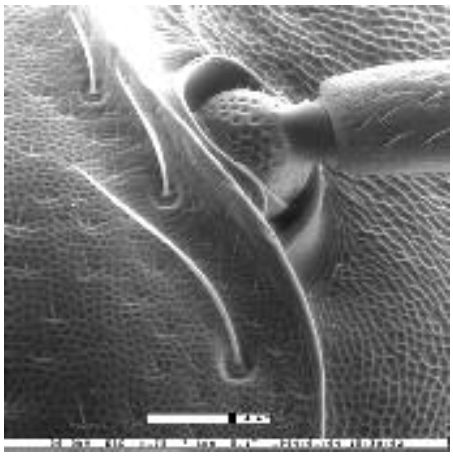
Environmental Scanning Electron Microscope	Biological ESEM Image of an Ant Head
	

Figure 4.3: Environmental Scanning Electron Microscope and sample biological image

4.2 REPRESENTITIVE FAILURE INSTANCES

As prescribed by the failure analysis hierarchal plan, every TV-1R test vehicle was examined for failures preceding the data analysis regimen. Two characteristically different failure types were apparent upon visually inspecting Gould and MacDermid boards. Failed MacDermid embedded resistors contained lightening discolorations in circular and rectangular shapes within the resistor material as illustrated in Figure 4.4a. Meanwhile, failed Gould embedded resistors contained darkening discolorations in thin and thick jagged lines as illustrated in Figure 4.6a. After visually inspecting failure sites, one test vehicle from each qualification experiment of each embedded resistor technology was further examined under the SAM using both through transmission and pulse echo inspection modes. The SAM revealed possible delaminating regions between the embedded resistors and FR-406 material within MacDermid test vehicles. Figure 4.4 (b), (c) and (d) illustrate the most egregious instance of MacDermid resistor delamination.

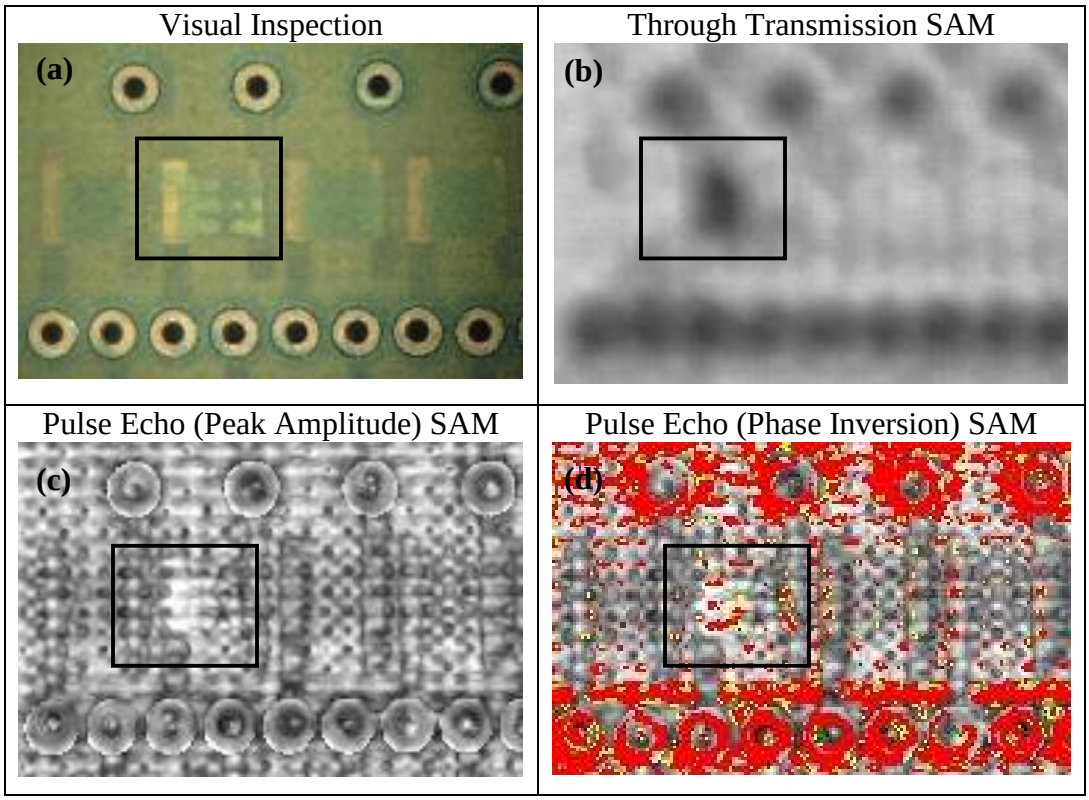


Figure 4.4: Optical and SAM imaging representing MacDermid resistor delamination

Conducting a through transmission C-scan revealed a large black splotched region indicating material inconsistency through the thickness of the PWB test vehicle at the location of an embedded resistor. Performing a pulse echo, peak amplitude C-scan at the embedded resistor revealed a corresponding white splotched region above the same location as the through transmission image signifying density changes at the resistor level. An additional pulse echo, phase inversion C-scan overlaid the white splotches in the peak amplitude image with red and yellow colorations indicating a phase change confirming material inconsistency above or below the embedded resistor. In order to pinpoint the failure mechanism, the embedded resistor was subsequently sectioned according to Level III destructive PWB sectioning techniques and observed under the

ESEM to investigate the failure mode. Delamination occurred between the embedded resistor and the subsequent FR-406 inner layer pair illustrated in Figure 4.5, images of both “good and “bad” embedded resistors making contact with either a left or right trace. As a result, the value of the embedded resistor increased approximately 1255% from 52Ω to 705Ω.

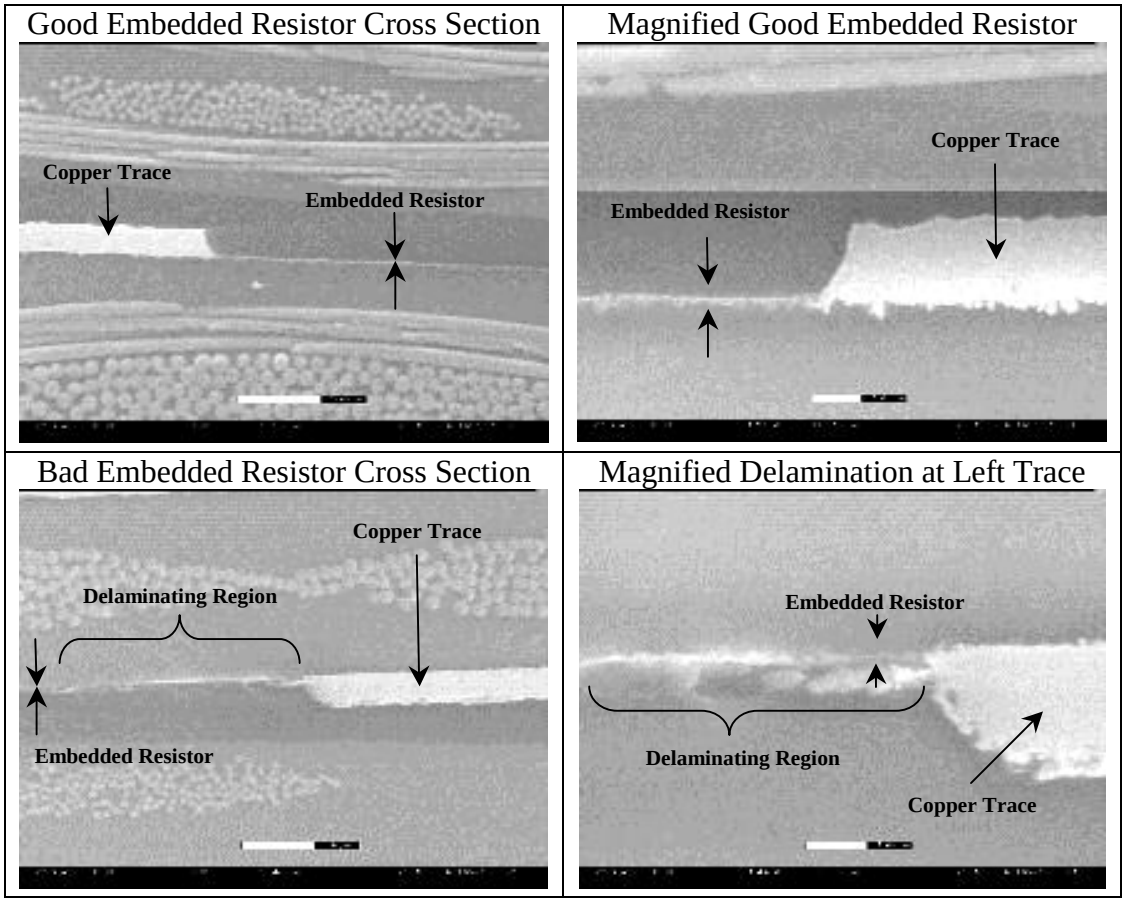


Figure 4.5: ESEM images of a “good” and “bad” MacDermid embedded resistor delaminating from an FR-406 inner layer

The SAM also revealed material inconsistencies within the Gould test vehicles; however, in a very different nature than those found within the MacDermid boards.

Figure 4.6 (b), (c) and (d) illustrate the most egregious failure instance within the Gould sample population. The boxed region in the optical image provided by Figure 4.6a suggests the occurrence of a failure phenomenon; however, upon examining the through transmission C-scan of the site, no additional information could be determined about the failure mechanism. Meanwhile, conducting a pulse echo, peak amplitude C-scan at the resistor level disclosed the possibility that the darkening region within the resistor was a metallic growth between copper traces either above or below the embedded resistor. In order to confirm the possibility, a pulse echo, phase inversion C-scan was performed. As expected, the corresponding darkened region in the optical image was overlaid with the red and yellow colorations suggesting material inconsistency at the resistor level. Moreover, the same red and yellow patterning was present throughout the copper traces on the rest of the TV-1R board suggesting the metallic growth was possibly copper, due to the similarities. In order to pinpoint and confirm the metallic growth hypothesis, the embedded resistor was sectioned according to Level III destructive PWB sectioning techniques and observed under an optical microscope. Metallic growth did occur between traces on the upper surface of the embedded resistor. Figure 4.7a provides an optical image of a "good" resistor while images (b), (c) and (d) illustrate the "bad" resistor investigated with the optical microscope. Likewise, Figure 4.8 provides further investigation with ESEM imaging. Looking more closely at the left and right traces, it is difficult to conclude that the metallic growth started from both traces equally since more of the copper builds at the right trace and thins as it approaches the left. In addition, since the resistor was the product of the temperature/humidity qualification test and no bias was used during testing, it cannot be concluded that a current flow starting from the right

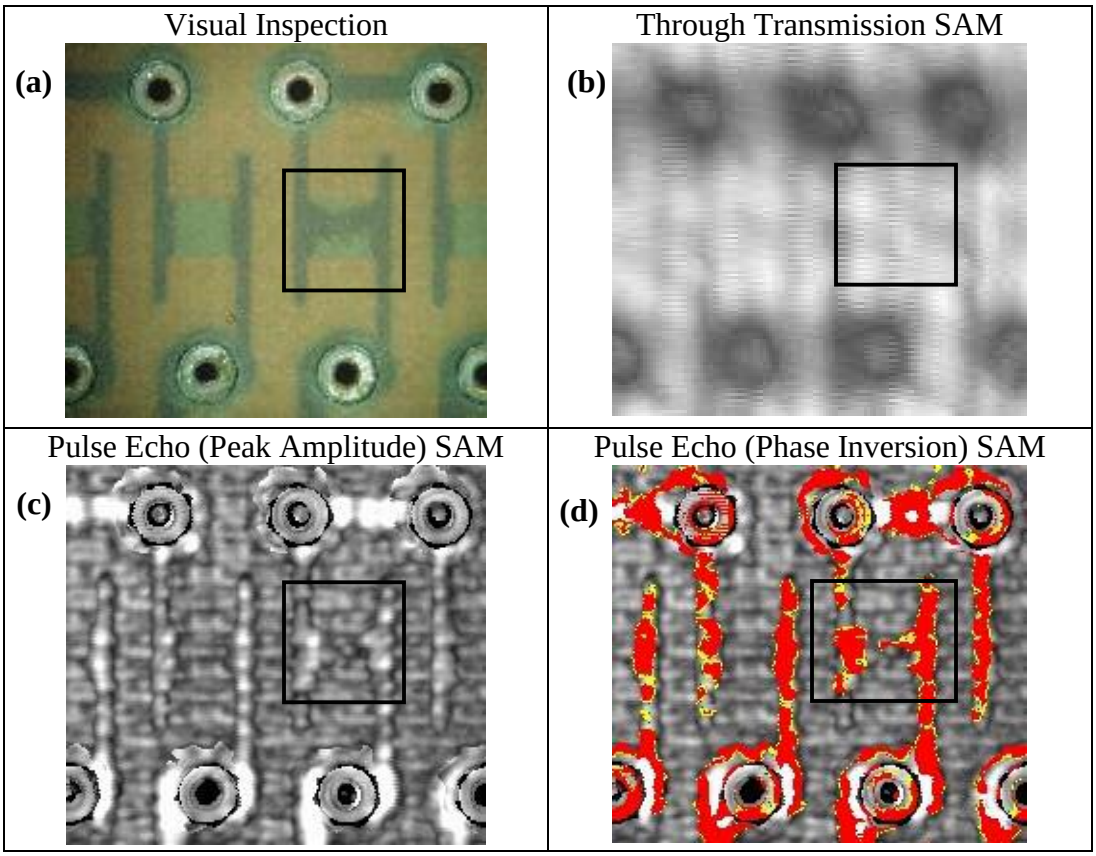


Figure 4.6: Optical and SAM imaging of a Gould embedded resistor

trace and ending at the left caused the thinning effect on the growth. The only possibility could be that during the measurement phase of the test plan, the copper traces were still malleable and the resulting current flow produced by the data acquisition equipment caused the transfer of copper as the resistance dropped and the current increased. In any instance, the value of the embedded resistor decreased almost 100% from 52Ω to 0.01Ω representing a short circuit.

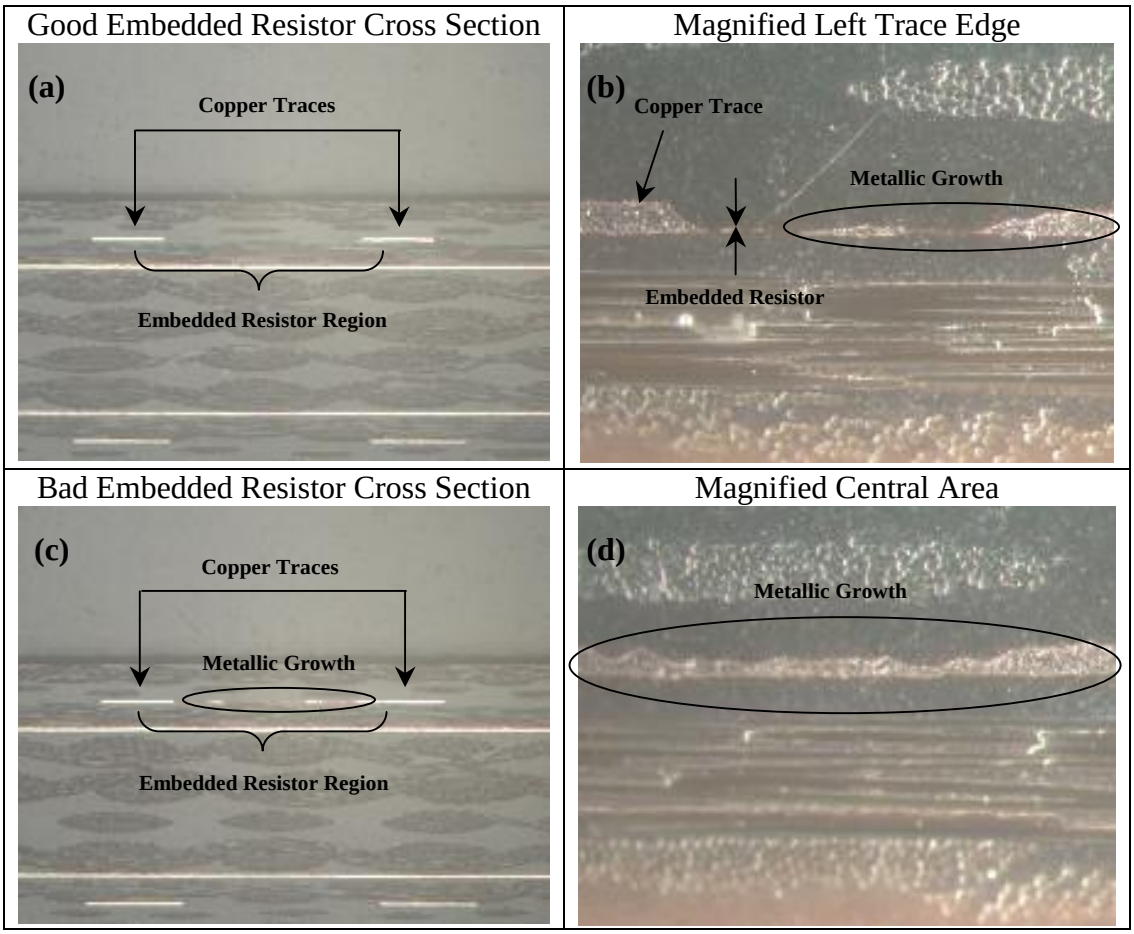


Figure 4.7: Optical images of a "good" and "bad" Gould embedded resistor demonstrating metallic growth

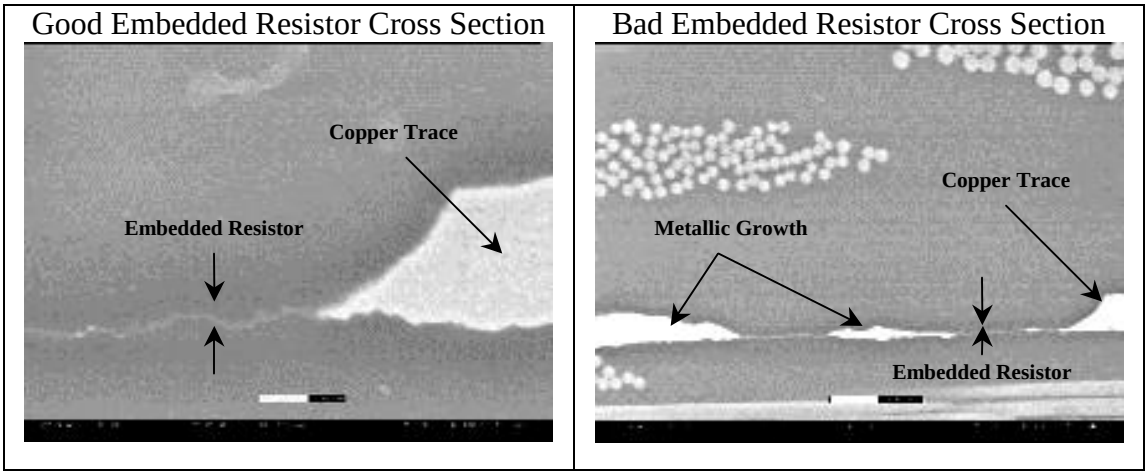


Figure 4.8: ESEM images of a "good" and "bad" Gould embedded resistor illustrating metallc growth

4.3 SUMMARY

While not all of the failure instances are illustrated, the remainder of the Gould and MacDermid sample populations exhibited the same types of failure mechanisms demonstrated in Section 4.2. While MacDermid embedded resistors exhibited delamination above the devices between the nickel phosphate resistor material and FR-406 inner layer increasing resistive value, Gould embedded resistors indicated decreasing resistive value as the result of metallic growth on the upper surface of the nickel chromium resistor material between copper traces. Accordingly, referring back to Chapter 3 and Appendix B, the majority of the Gould histograms represent negatively weighted distributions signifying decreases in resistance. In the same manner, the majority of MacDermid histograms represent positively weighted distributions signifying increases in resistance. A correlation between the distribution of resistance values illustrated within the data analysis histograms and the observed failure mechanisms on the embedded resistors can be concluded.

CHAPTER 5 SUMMARY

5.1 CONCLUSION

The experimental results obtained through strategically selected environmental qualification experiments were used to determine the operating characteristics and failure mechanisms associated with Gould's subtractive nickel chromium and MacDermid's additive nickel phosphorous embedded resistor technologies used in printed wiring boards. In addition, the embedded resistors were inspected for and found to be insensitive to configuration in horizontal/vertical orientations, reworked/non-reworked conditions and isolated/daisy chained connections. Furthermore, Gould's subtractive technology has proven to be an order of magnitude more stable than MacDermid's additive technology. Table 5.1 provides a summary of the results obtained for the entire sample population. While the majority of Gould's resistors responded to environmental stressing with decreasing resistive values, the majority of MacDermid's resistors responded with increasing resistive values. Gould failures were the result of metallic growth on the upper surface of the embedded resistor meanwhile MacDermid failures were the result of delamination between the upper surface of the embedded resistor and the FR-406 inner layer. Both technologies failure mechanisms could possibly be diminished using tighter tolerance manufacturing constraints to eliminate unnecessary defects that historically lead to delamination and metallic growth. Cleaner, smoother substrate surfaces, more adhesive bonding methods, additional annealing processes, more pure, untarnished materials, etc. could also all help to alleviate these unwanted defects. Even though Gould and MacDermid's technologies have less tolerance adherence than

Table 5.1: Summary of Experimental Results

Qualification Experiment	Manufacturer					
	Gould			MacDermid		
	Expected shift in resistance	σ	Failures*	Expected shift in resistance	σ	Failures*
Lamination (Pre/Post)	2.4%	6.54	0	-1.92%	1.27	0
Temperature Coefficient of Resistance (-25°C to 125°C at 0.625°C /min)	205.02**	37.56	0	-13.89 **	26.01	0
Stabilization Bake (105°C after 2400 hours)	0.78%	3.81	3	2.36%	3.05	0
Temperature Cycling (-65°C to 125°C at 5°C/min, 30 min dwell at extremes after 500 cycles)	0.91%	4.40	2	1.58%	2.96	1
Thermal Shock (-40°C to 120°C, 5 min dwell at extremes after 500 cycles)	1.68%	4.36	1	2.76%	3.71	0
Temperature/Humidity (130°C with 85% RH at 2.235atm after 1244 hours)	6.74%	8.80	47	27.77%	13.56	29
Embedded Resistor Technology	Subtractive Nickel Chromium			Additive Nickel Phosphorous		
Failure Mechanism	Metallic Growth			Delamination		

*Failures defined as $\Delta R > 50\%$ **Temperature Coefficient of Resistance (ppm/°C)

highly developed high precision surface mount discrete resistor technologies (approximately 2 orders of magnitude), embedded resistors will undoubtedly establish themselves in the high speed electronic systems market since they have proven to eliminate almost all of the inductance, and thus reactance, normally associated with discrete resistors and their vias.

5.2 CONTRIBUTIONS

- Performed first extensive reliability study on embedded resistors. Previous (smaller scale) studies did not include trimmed resistors and resistors that have been reworked.
- Developed an accelerated environmental qualification test plan to obtain the thermal characteristics and reliability of both Gould and MacDermid embedded resistor technologies in various configurations including size, orientation, isolated/daisy chained connection, inkjet reworked/not reworked and/or laser trimmed.
- Conducted a three level, hierarchical failure analysis to extract failure modes and mechanisms responsible for altering embedded resistance value within a printed wiring board.
- Provided statistical and time-dependant representations to illustrate the differentiating effect of harsh environments on various configurations of additive nickel phosphate and subtractive nickel chromium embedded resistors.

- Developed a dynamic data acquisition method to sample TV-1R test vehicles in both real-time and post-experiment arrangements.
- Reported the effect of press lamination during the manufacturing process on various configurations of Gould and MacDermid embedded resistor technologies.

5.3 FUTURE WORK

Currently, another group of TV-1R test vehicles are being environmentally stressed under biased conditions and subjected to an appropriate failure analysis methodology. In addition, another sample group is also being environmentally stressed under 85% relative humidity (RH) at 85^{o}C in order to validate the results achieved through the highly accelerated temperature/humidity regimen conducted in the HAST chamber (85% RH at 130^{o}C under 2.235atm). Consequently, the next phase of characterization for the embedded resistors should focus on mechanically stressed conditions including bending and torsion schemes. Additionally, both a mathematical representation and finite element model needs to be developed. Moreover, different environmental and mechanical stress levels should be addressed to asses a failure rate to compare with an actual operating field failure rate to develop an analytical model predicting embedded resistor reliability. Finally, supplementary failure inspection is necessary to determine what design constraints are responsible for the failure mechanisms exhibited within Gould and MacDermid embedded resistor technologies to provide design enhancements improving performance, tolerance levels and ultimately reliability.

APPENDIX A EMBEDDED RESISTOR AND CAPACITOR MATERIALS

Table A.1: Generic list of embedded resistor materials [McGregor 2001]

Passive Type	Organic/ Inorganic	Passive Material Composition	Material Thickness (micron)	Description of Material as Supplied to Fabricator	Description of Material in Finished PWB
Resistor	I	Nickel/phosphorus	Less than 1 micron. Thickness is adjusted to obtain desired sheet resistivity.	Thin film nickel/phosphorus deposited on copper foil. Copper foil is laminated, resistor side in, to single sided FR-4 or other laminate.	Nickel/phosphorus layer connects two copper conductors to create a path of high resistance. The resistor material remains under all copper that remains on the board and is removed from all areas of the board that have no copper except in the areas where resistor elements are desired.
Resistor	I	Lanthanum boride ceramic	10 - 15	Paste. Or, a laminate with ceramic resistor elements fired on copper foil in pre-determined locations and laminated, resistor side in, to single sided FR-4 core.	Resistor material is located between imaged copper conductors. Imaging is done by fabricator.
Resistor	O	Resistor encapsulant paste Ceramic filled epoxy	10 - 15	Paste applied after firing the resistor paste, K1, and then cured. This is done before laminating, resistor side in, to single sided FR-4 core. Encapsulant paste extends beyond resistor to include circuit terminations.	Resistor materials K1 and K2 are located between imaged copper terminations. Imaging of termination circuitry is done by fabricator.

Passive Type	Organic/ Inorganic	Passive Material Composition	Material Thickness (micron)	Description of Material as Supplied to Fabricator	Description of Material in Finished PWB
Resistor	O	Resistor encapsulant paste Ceramic filled epoxy	10 - 25	Paste applied by fabricator following imaging of embedded resistor laminate, K1.	Protective encapsulant applied over resistor, K1, opposite encapsulant K2. Encapsulant K3 will be surrounded by cured prepreg after multilayer lamination.
Resistor	O	Metal oxides in polyimide	20 - 25	Paste. Paste applied to imaged circuit terminations and cured by fabricator.	Resistor material is located between imaged copper conductors encapsulated by prepreg during multilayer lamination.
Resistor	I	Nickel/phosphorus	0.1	Nickel/phosphorus plating chemistry.	Fabricator plates nickel/phosphorus between pre-imaged conductors to create resistor elements.
Resistor	I	Platinum alloy	< 0.2	Thin film platinum alloy on copper foil, or laminated, alloy side in, to single sided core.	Platinum alloy layer connects two copper conductors to create a path of high resistance. The platinum alloy remains under all copper that remains on the board and is removed from all areas of the board that have no copper except in the areas where resistor elements are desired.

Passive Type	Organic/ Inorganic	Passive Material Composition	Material Thickness (micron)	Description of Material as Supplied to Fabricator	Description of Material in Finished PWB
Resistor	I	Nickel/chromium	0.01 - 0.03	Thin film nickel/chromium on copper foil, or laminated, nickel/chromium side in, to single sided core.	Nickel/chromium layer connects two copper conductors to create a path of high resistance. The nickel/chromium remains under all copper that remains on the board and is removed from all areas of the board that have no copper except in the areas where resistor elements are desired.
Resistor	I	Nickel/chromium/ aluminum/silicon	0.01 - 0.03	Thin film Ni/Cr/Al/Si on copper foil, or laminated, Ni/Cr/Al/Si side in, to single sided core.	Ni/Cr/Al/Si layer connects two copper conductors to create a path of high resistance. The Ni/Cr/Al/Si remains under all copper that remains on the board and is removed from all areas of the board that have no copper except in the areas where resistor elements are desired.

Table A.2: Generic list of embedded capacitor materials

Passive Type	Organic/ Inorganic	Passive Material Composition	Material Thickness (micron)	Description of Material as Supplied to Fabricator	Description of Material in Finished PWB
Capacitor	O	Glass reinforced epoxy	25 – 50	Laminate with copper on both sides of core.	Copper power and ground planes with glass/epoxy core.
Capacitor	O	Barium titanate filled polyimide	8 – 25	Laminate with copper on both sides of core.	Copper power and ground planes with filled polyimide core.
Capacitor	O	Barium titanate filled epoxy	4 – 25	Laminate with copper on both sides of core.	Copper power and ground planes with filled epoxy core.
Capacitor	O	Unfilled polyimide	12 – 25	Laminate with copper on both sides of core.	Copper power and ground planes with unfilled polyimide core.
Capacitor	I	Thin film silicon dioxide	< 2	Laminate with copper on both sides of core.	Copper power and ground planes with thin film silicon dioxide core.
Capacitor	I	Sintered barium titanate ceramic	10 - 25	Paste. Or, a laminate with the singulated capacitors fired on copper foil in pre-determined locations and laminated, capacitor side in, to single sided FR-4 laminate.	Ceramic dielectric with original copper foil as one electrode of the singulated capacitors and either a silver or copper based fired second electrode. The capacitors are encapsulated by the FR-4 laminated to the original copper foil. Fabricator imaging, drilling and plating provide connection to the two electrodes of the capacitor.

Passive Type	Organic/ Inorganic	Passive Material Composition	Material Thickness (micron)	Description of Material as Supplied to Fabricator	Description of Material in Finished PWB
Capacitor	O	Barium tiatante filled polyimide	10 - 25	Paste. Paste is applied to copper imaged by fabricator. The copper becomes one electrode. After curing, fabricator applies conductor paste, G2, and cures.	Barium titanate filled polyimide dielectric with laminate copper foil as one electrode of the singulated capacitors and either a silver or copper based cured second electrode. The singulated capacitors are encapsulated by prepreg during multilayer lamination. Fabricator imaging, drilling and plating provide connection to the two electrodes of the capacitor.

APPENDIX B ADDITIONAL EXPERIMENTAL RESULTS

Contained within Appendix B is the remainder of the figures illustrating aggregate embedded resistor response to the various environmental qualification test schemes segregated by configuration as well as selected case time-dependent studies. For the remainder of the experimental results, refer back to Chapter 3, Sections 3.2 through 3.7.

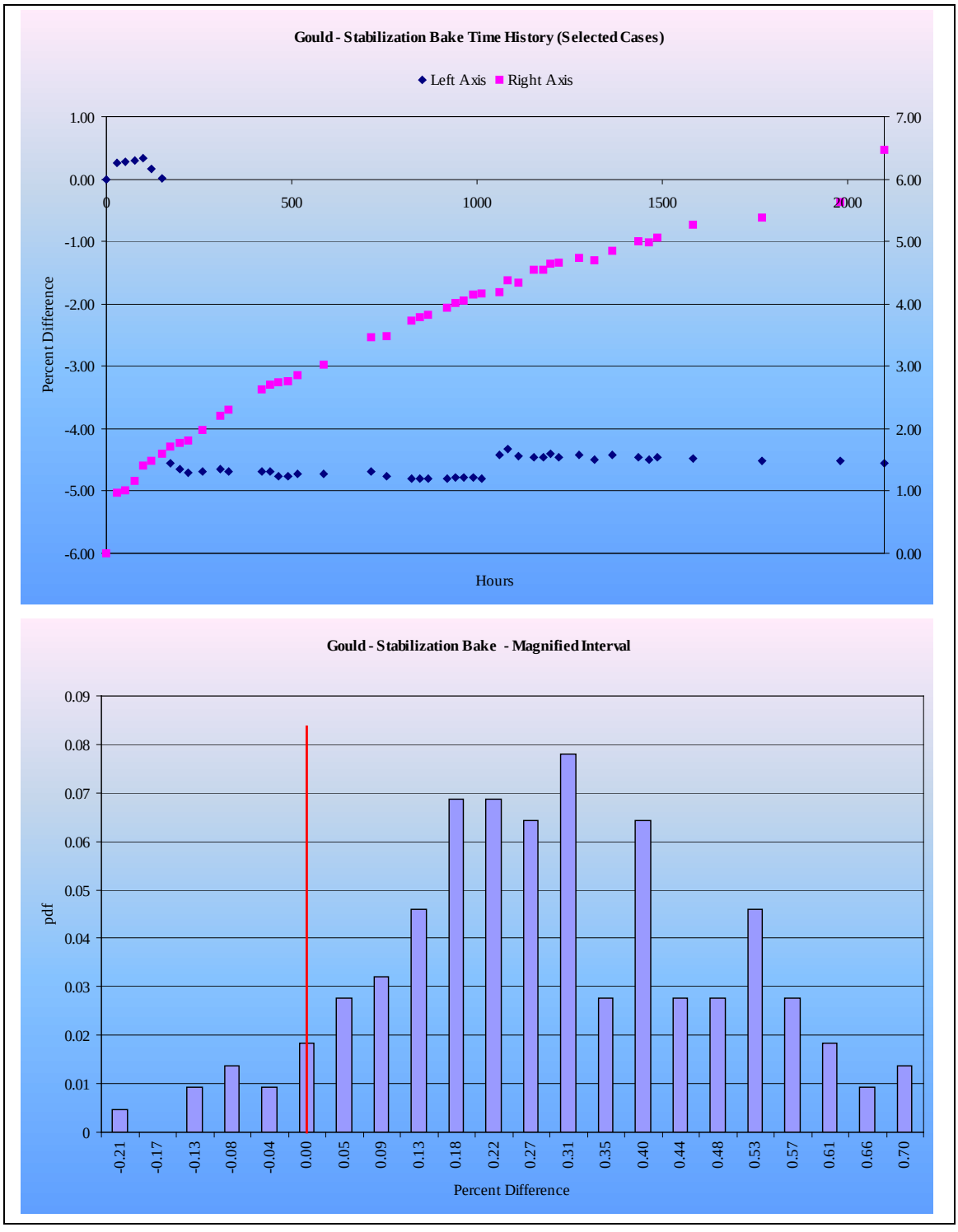


Figure B.1: Gould embedded resistor stabilization bake analysis after 2400 hours

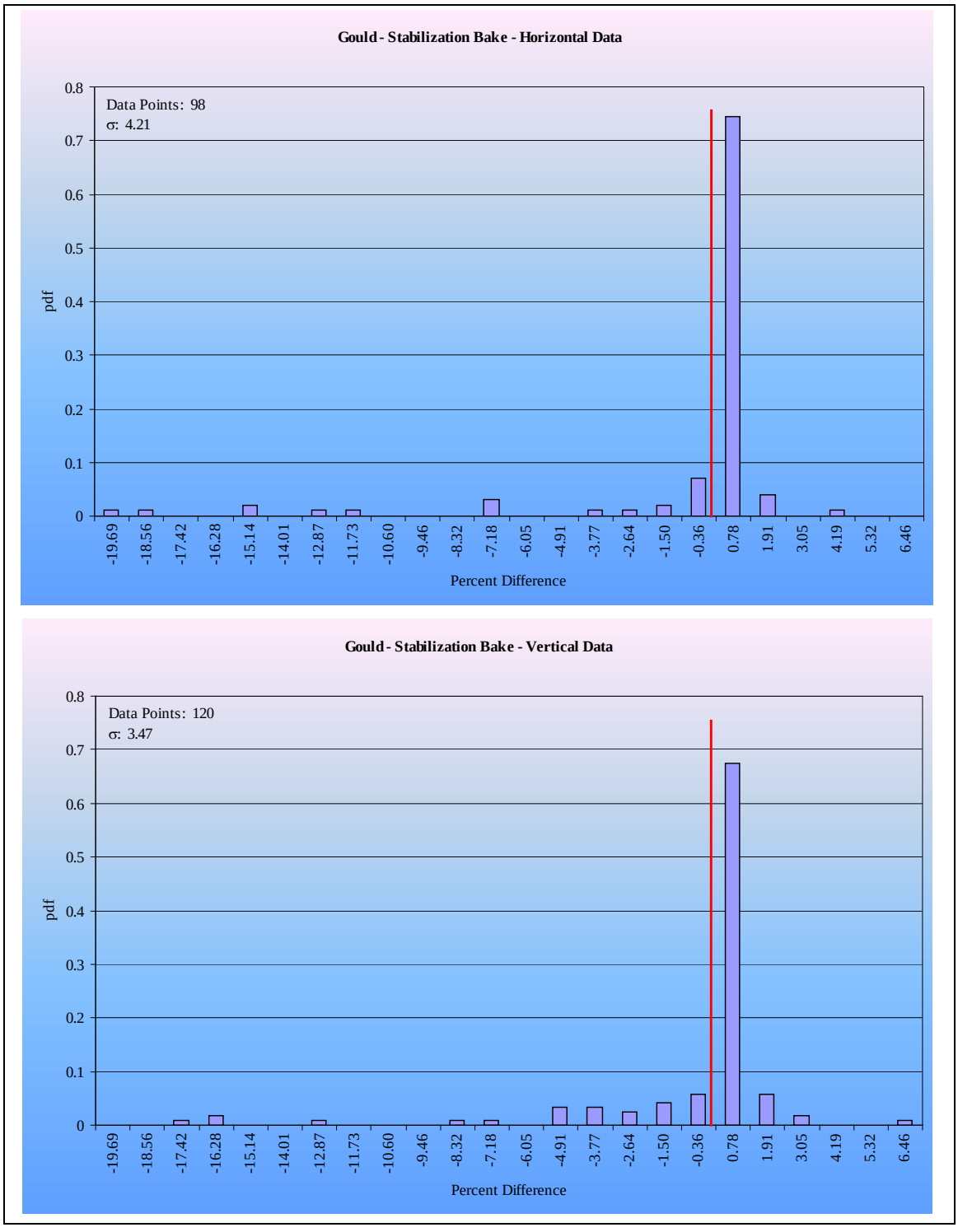


Figure B.2: Gould embedded resistor stabilization bake analysis after 2400 hours sorted by orientation

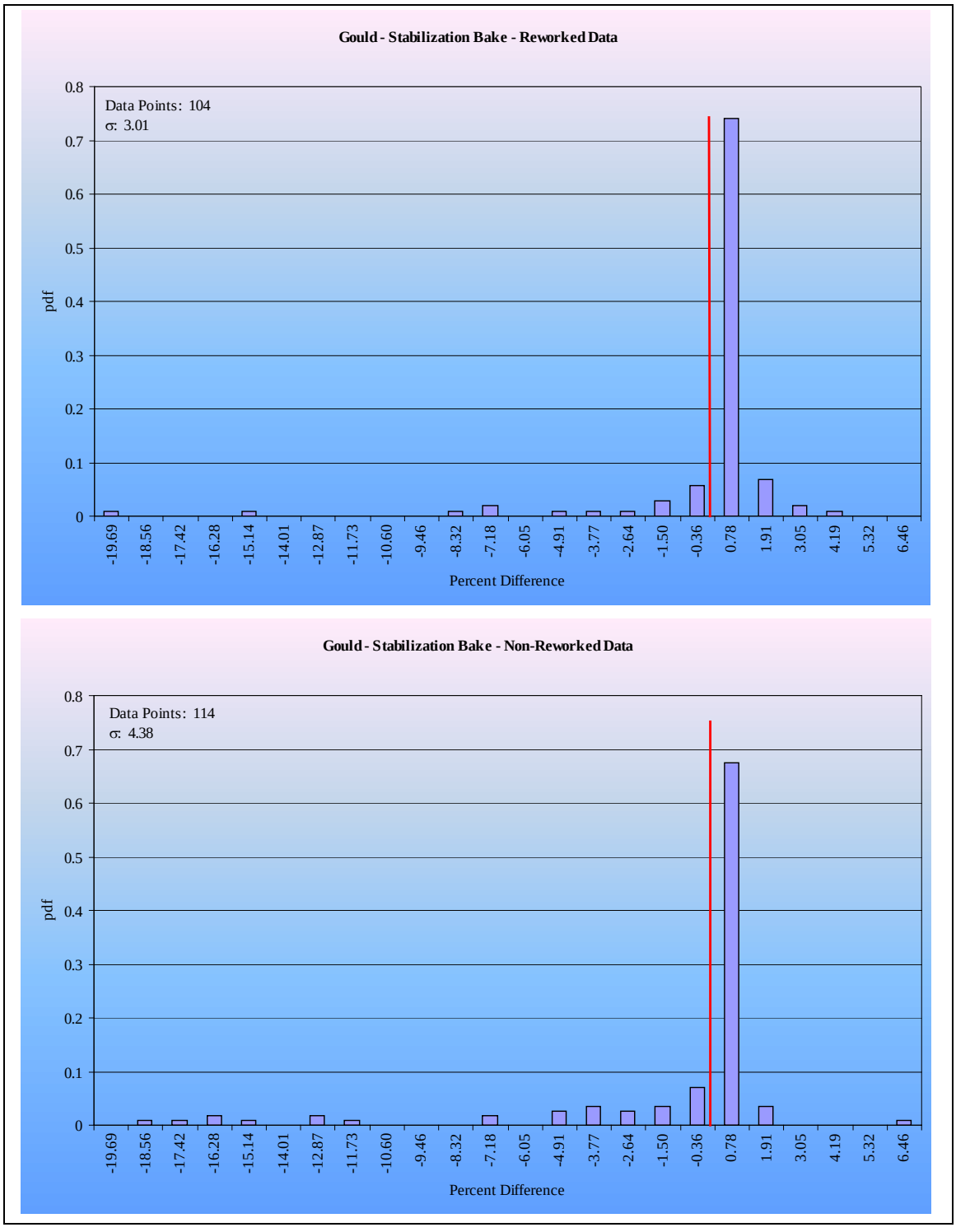


Figure B.3: Gould embedded resistor stabilization bake analysis after 2400 hours sorted by rework

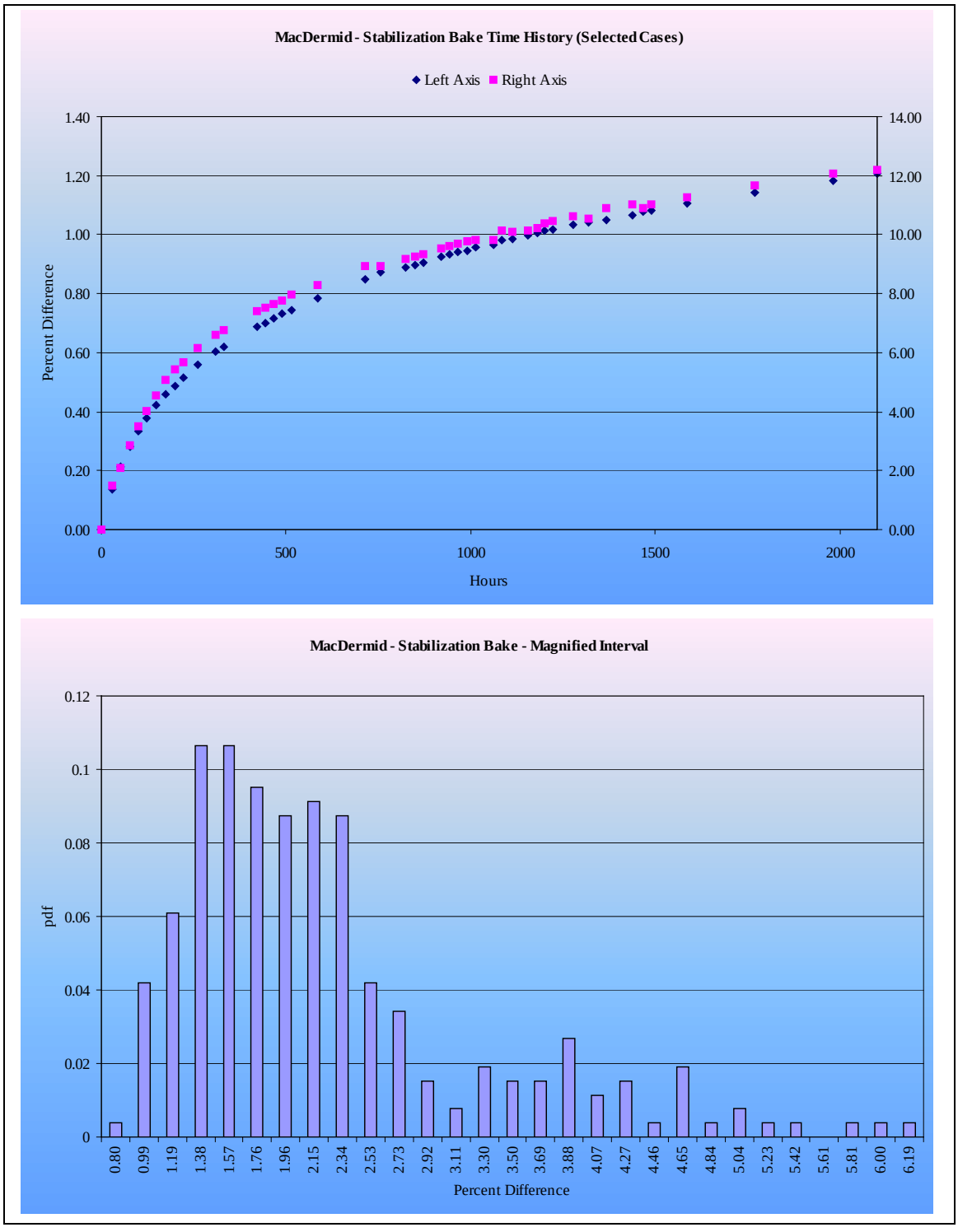


Figure B.4: MacDermid embedded resistor stabilization bake analysis after 2400 hours

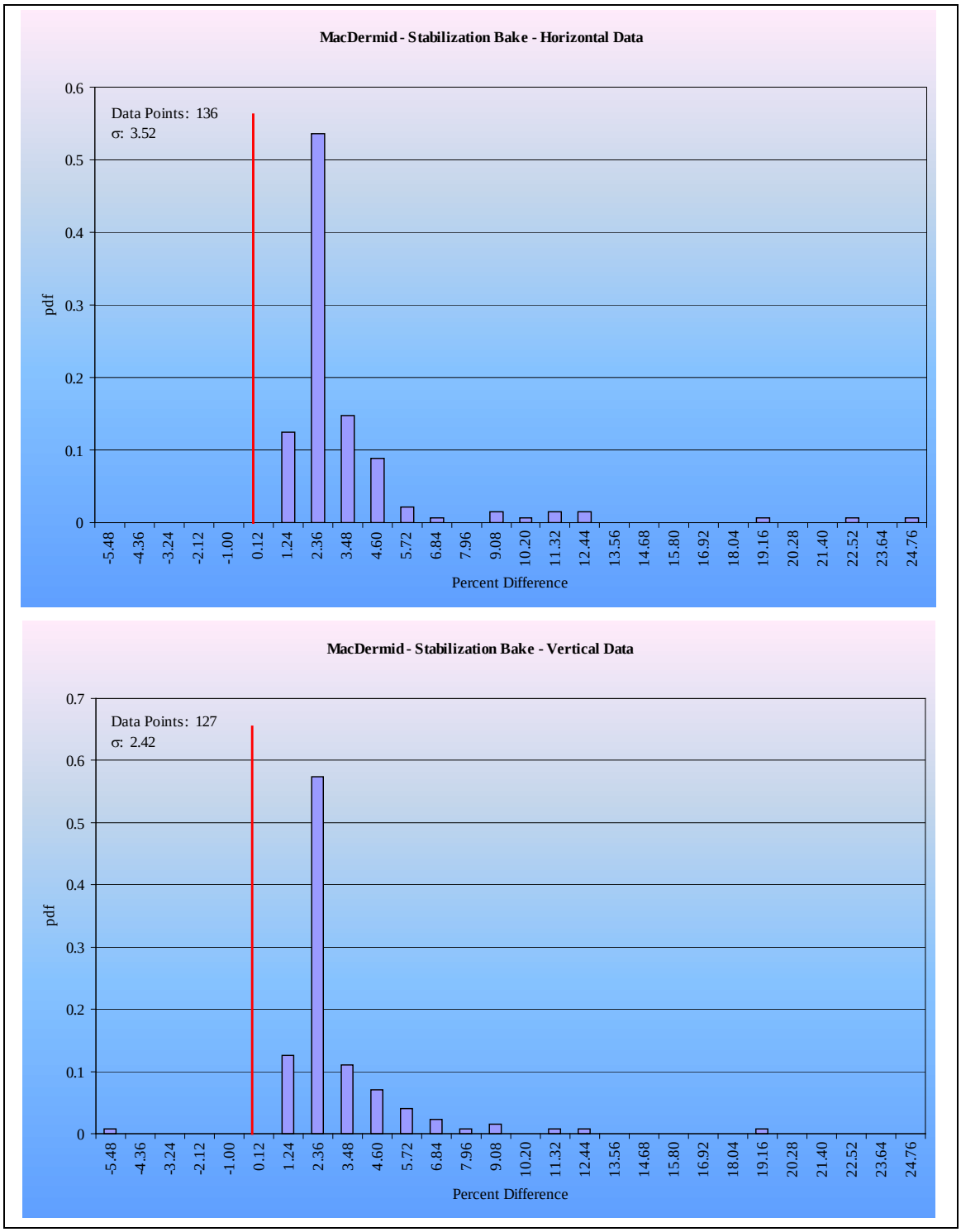


Figure B.5: MacDermid embedded resistor stabilization bake analysis after 2400 hours sorted by orientation

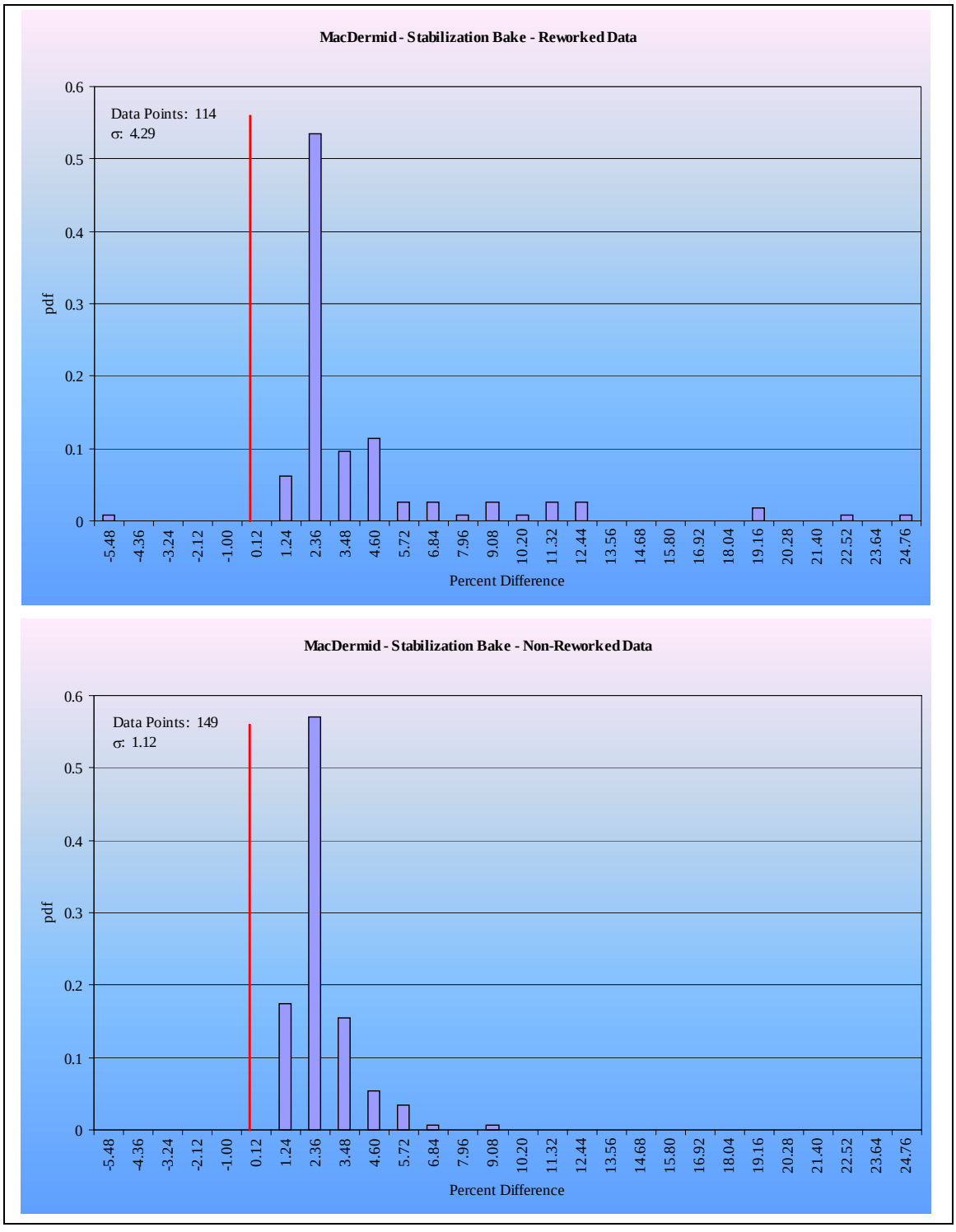


Figure B.6: MacDermid embedded resistor stabilization bake analysis after 2400 hours sorted by rework

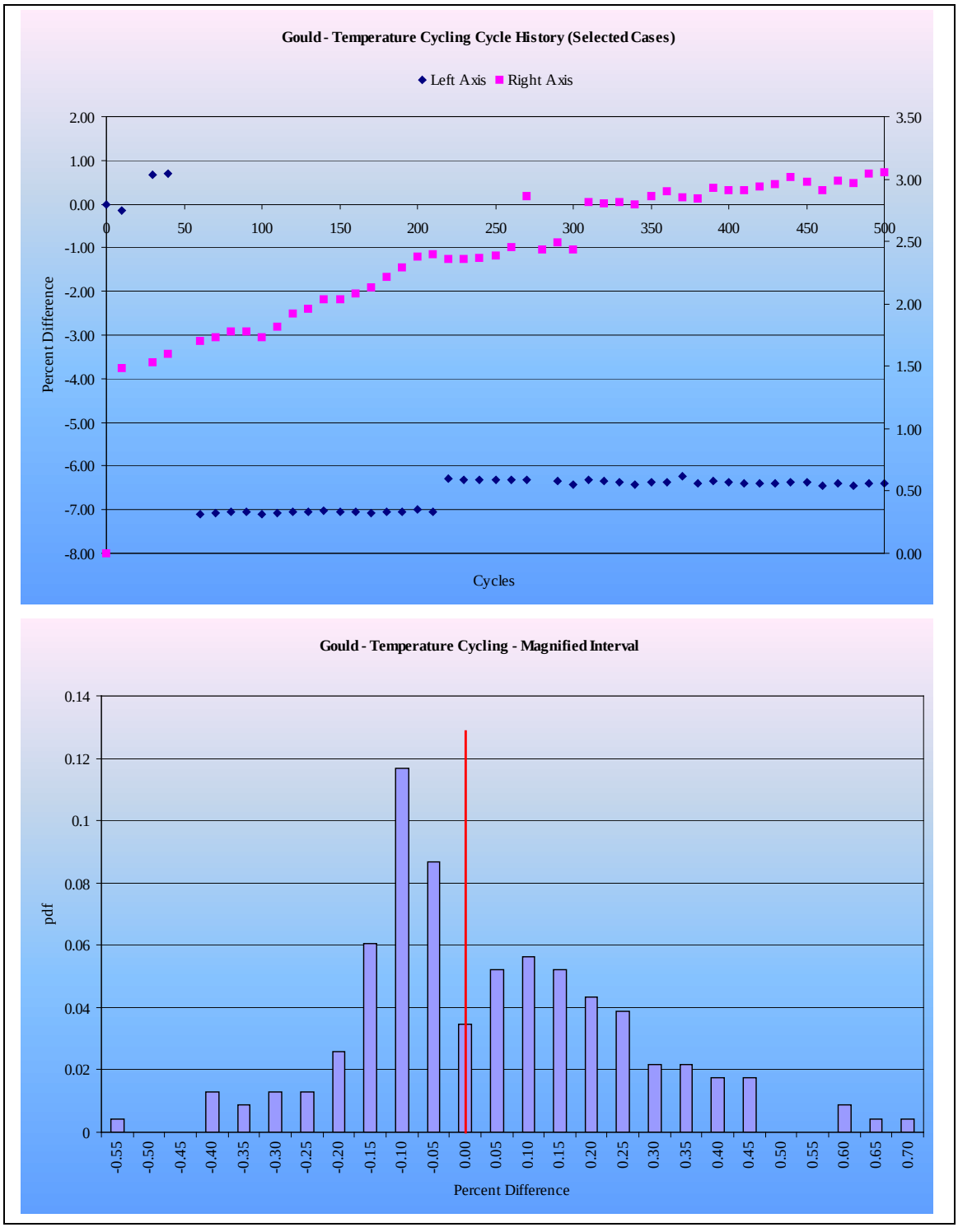


Figure B.7: Gould embedded resistor temperature cycling analysis after 500 cycles

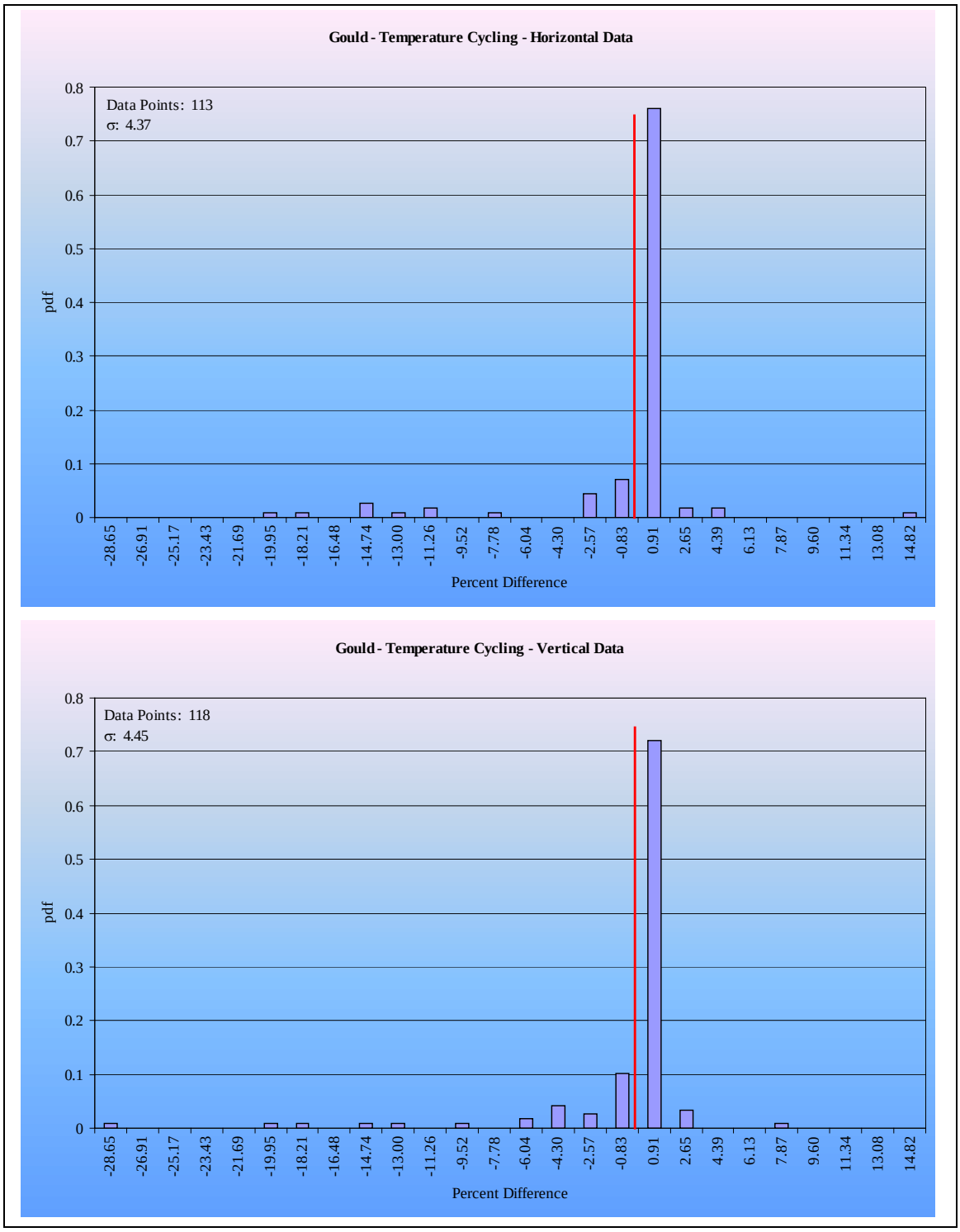


Figure B.8: Gould embedded resistor temperature cycling analysis after 500 cycles sorted by orientation

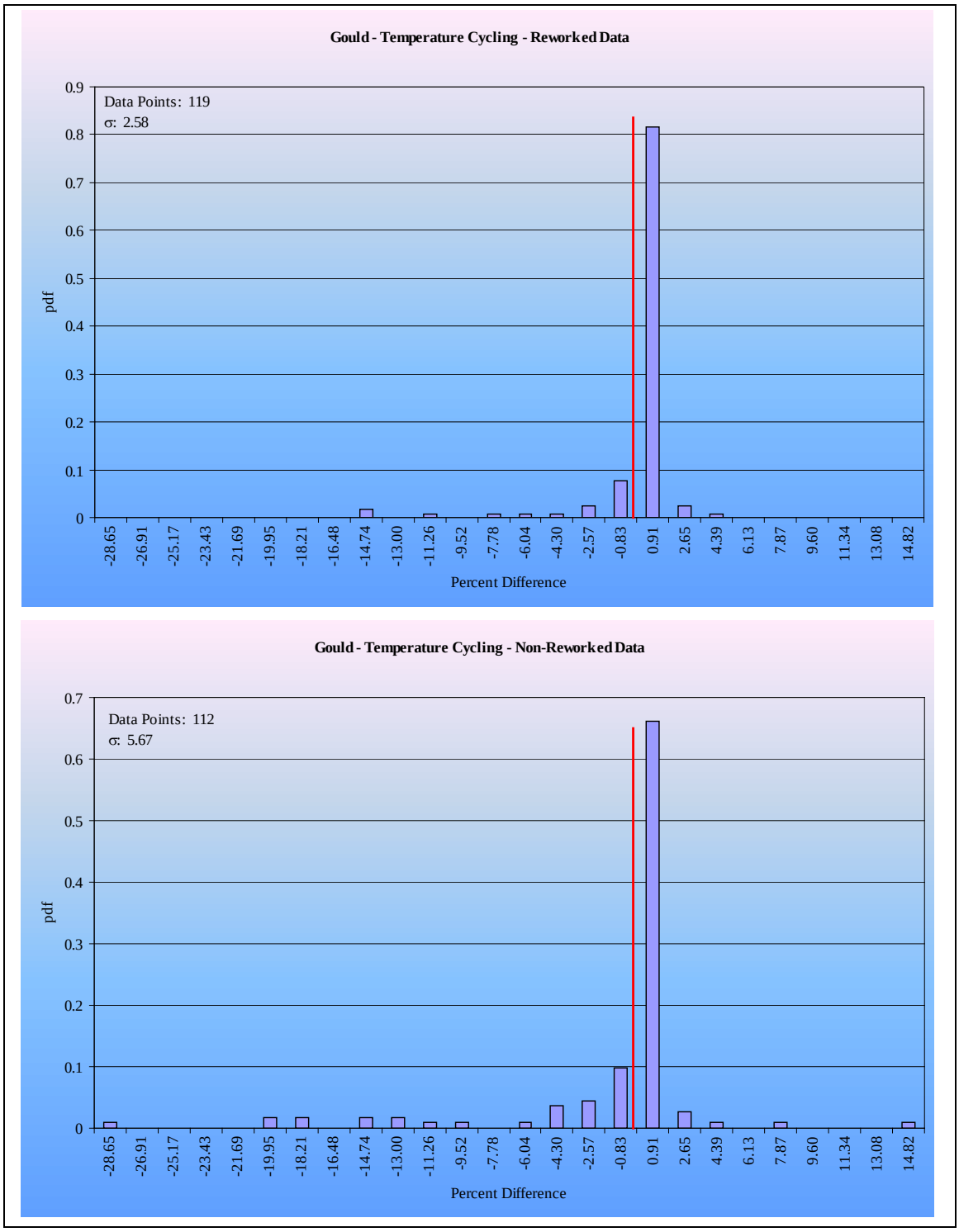


Figure B.9: Gould embedded resistor temperature cycling analysis after 500 cycles sorted by rework

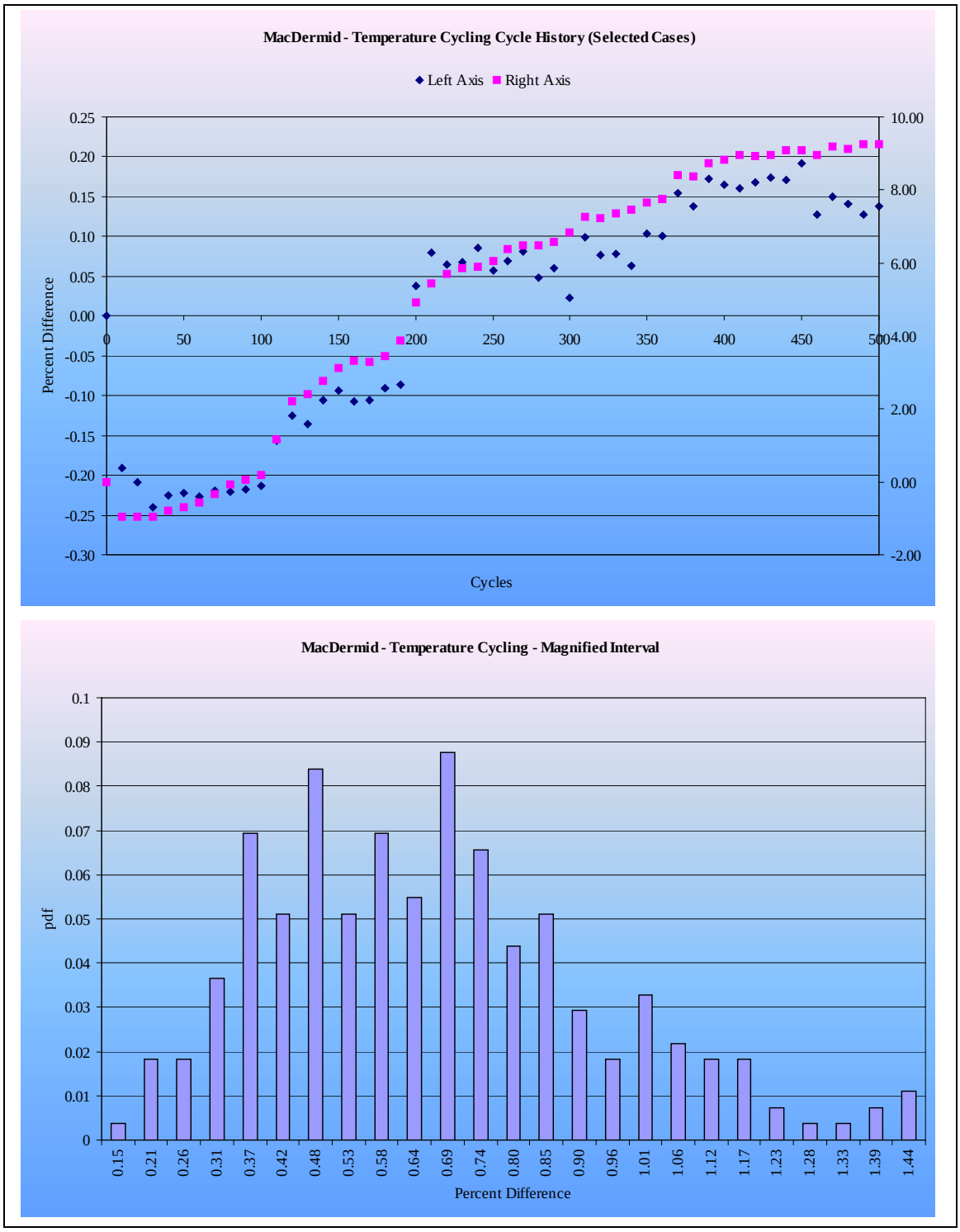


Figure B.10: MacDermid embedded resistor temperature cycling analysis after 500 cycles

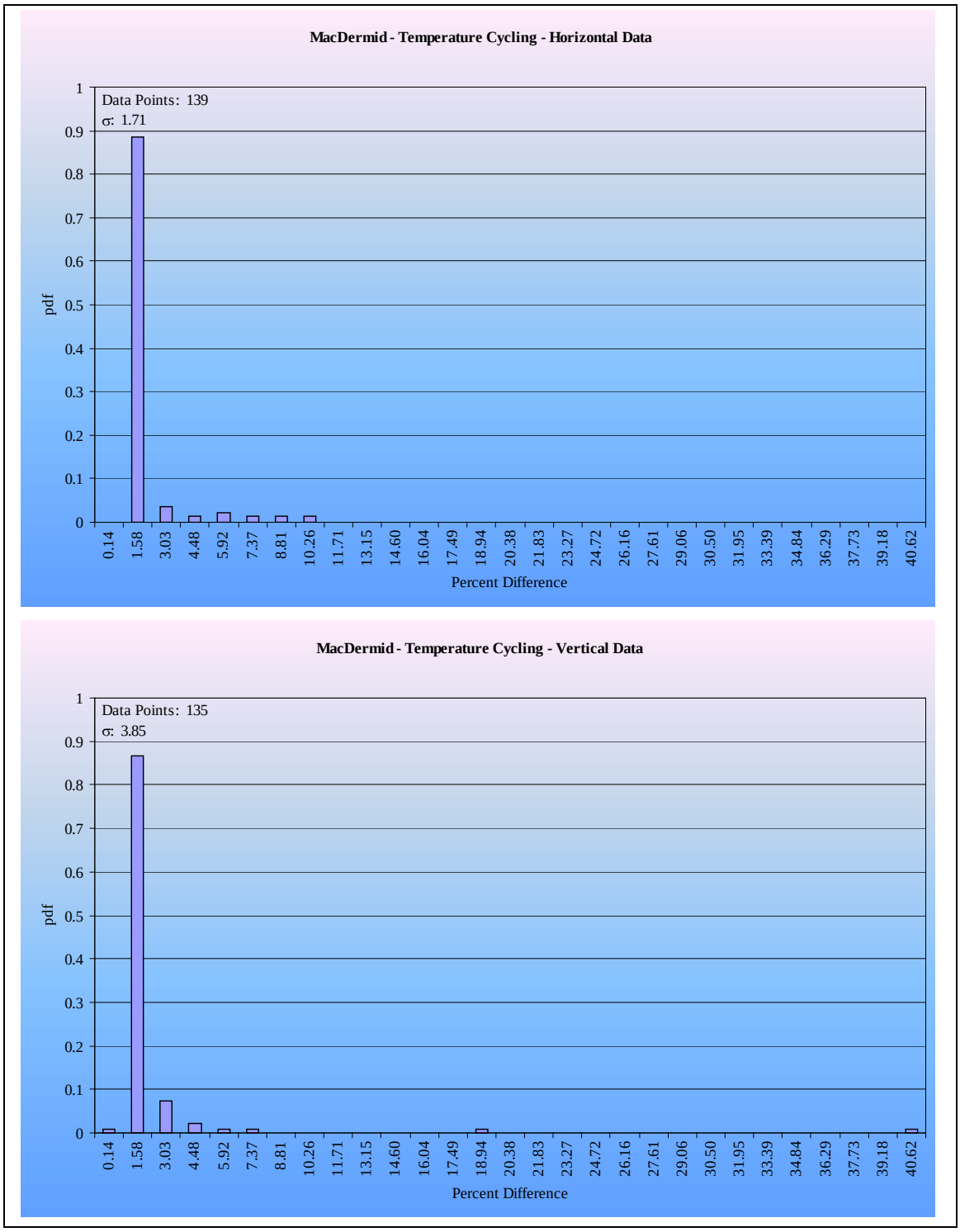


Figure B.11: MacDermid embedded resistor temperature cycling analysis after 500 cycles sorted by orientation

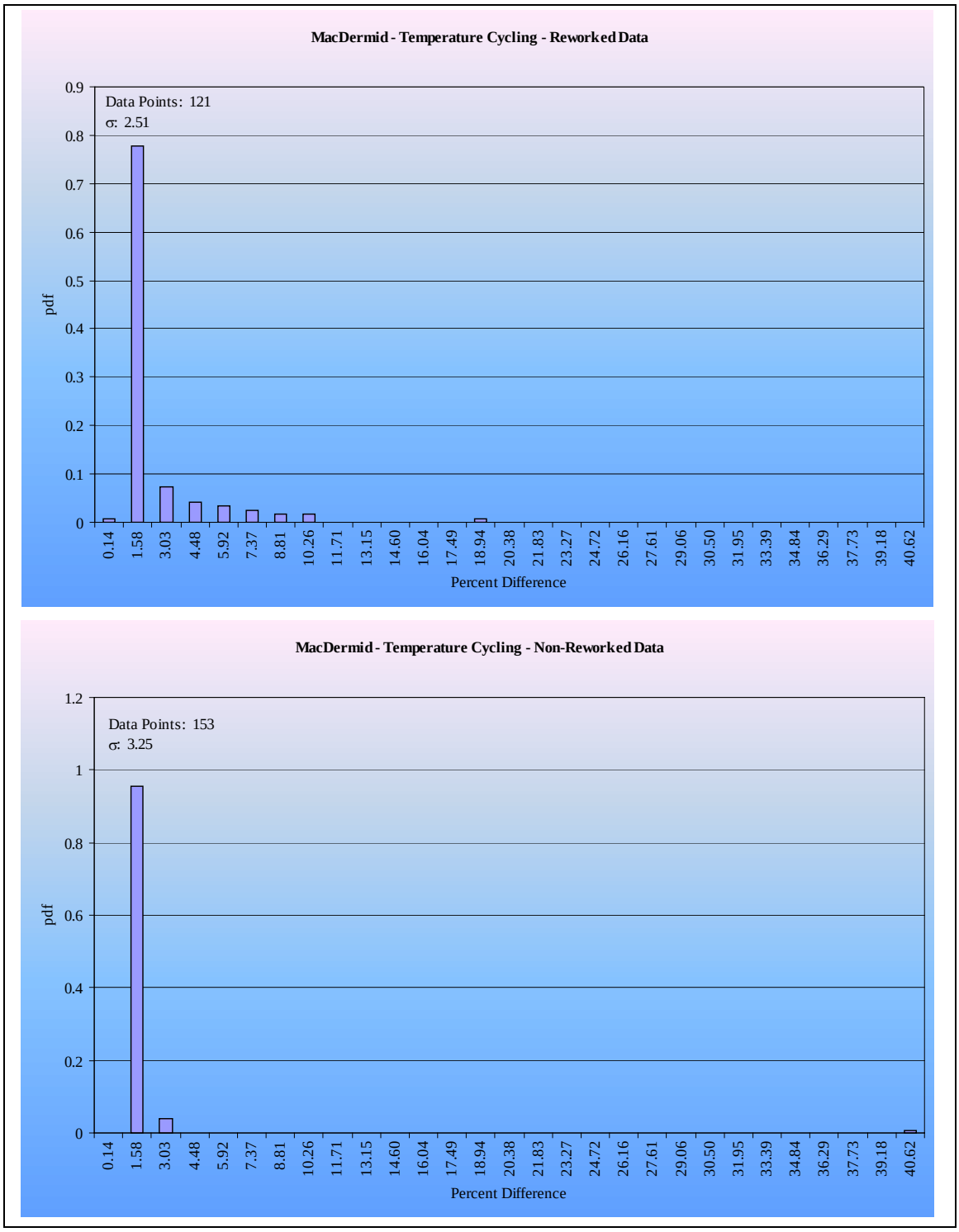


Figure B.12: MacDermid embedded resistor temperature cycling analysis after 500 cycles sorted by rework

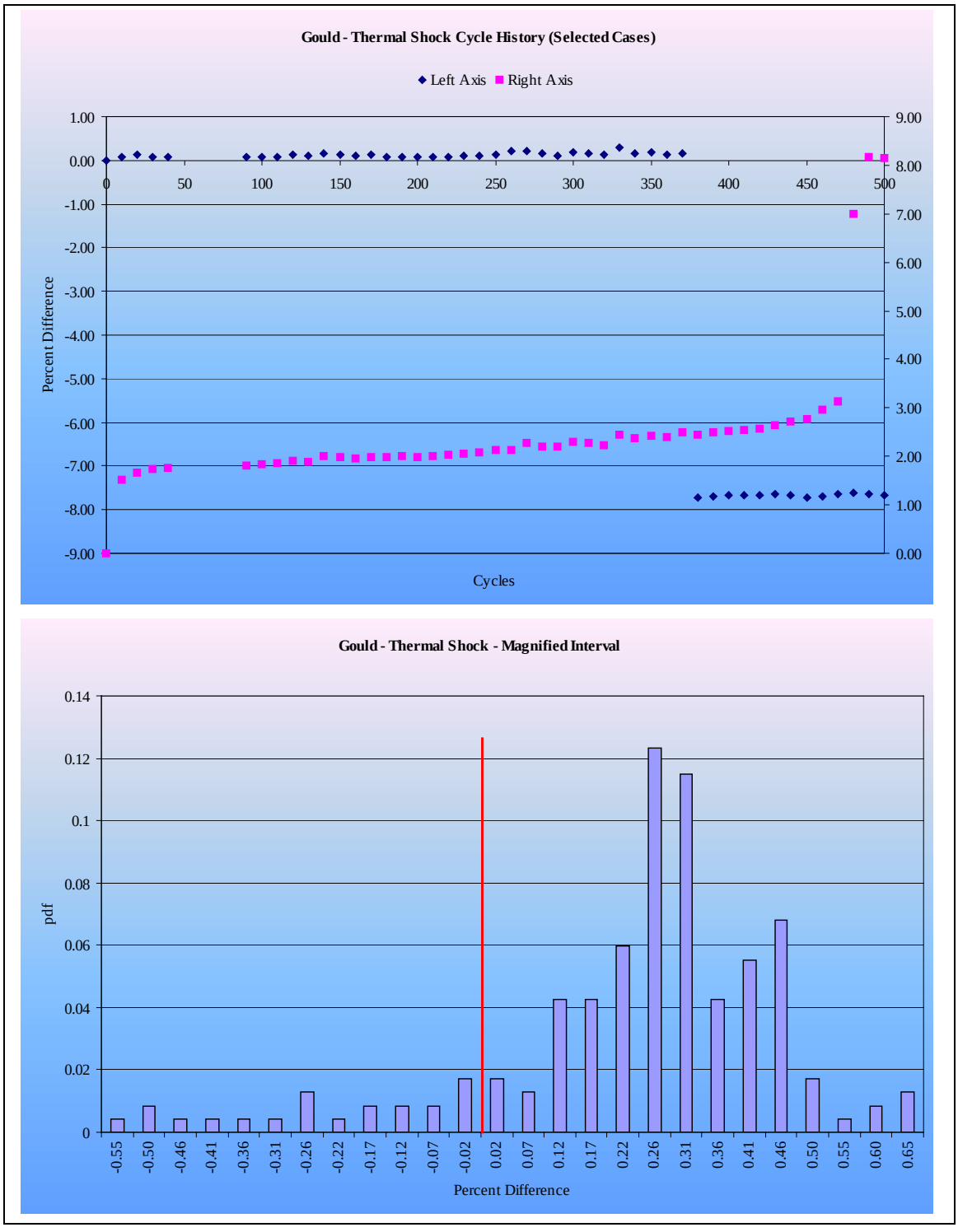


Figure B.13: Gould embedded resistor thermal shock analysis after 500 cycles

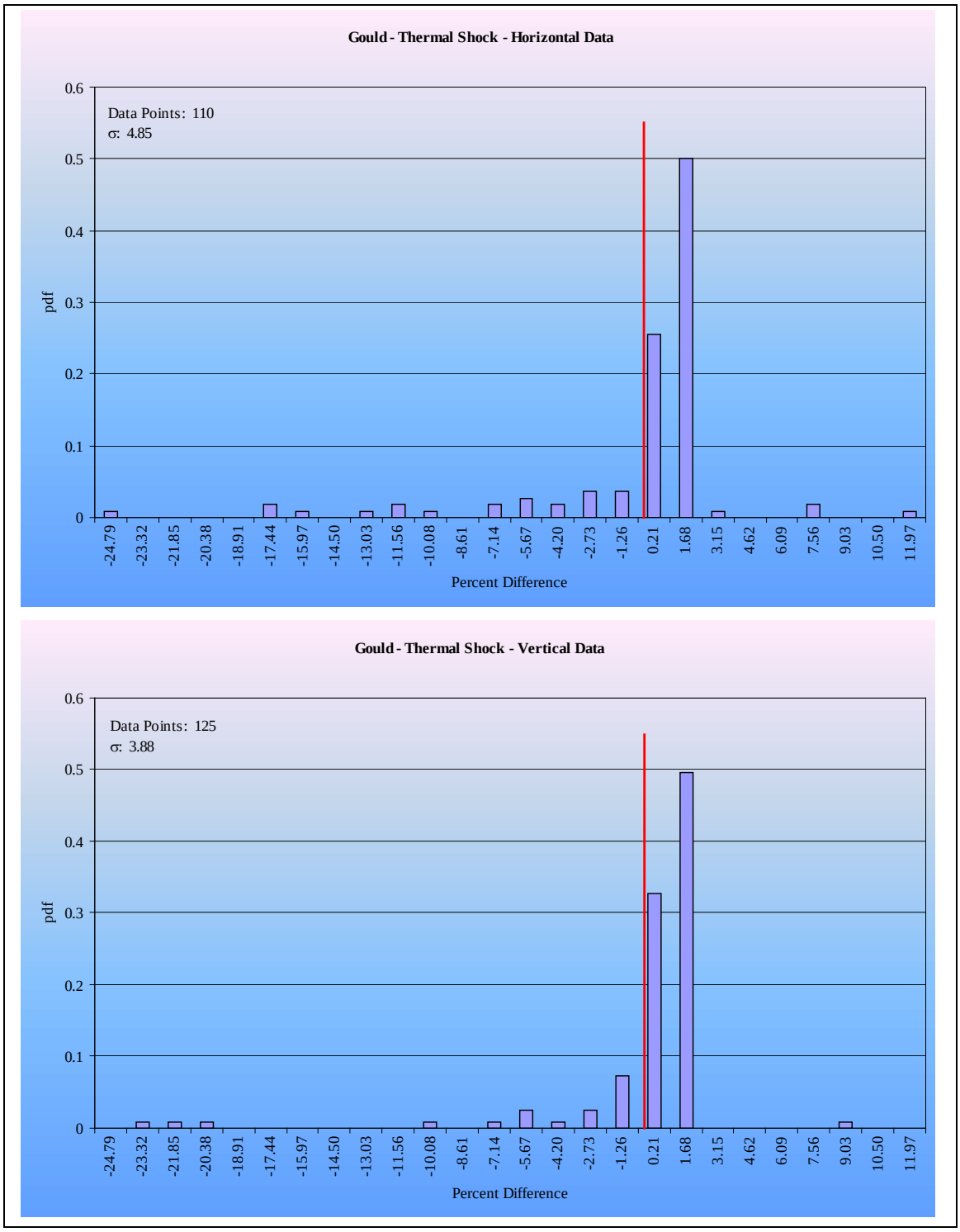


Figure B.14: Gould embedded resistor thermal shock analysis after 500 cycles sorted by orientation

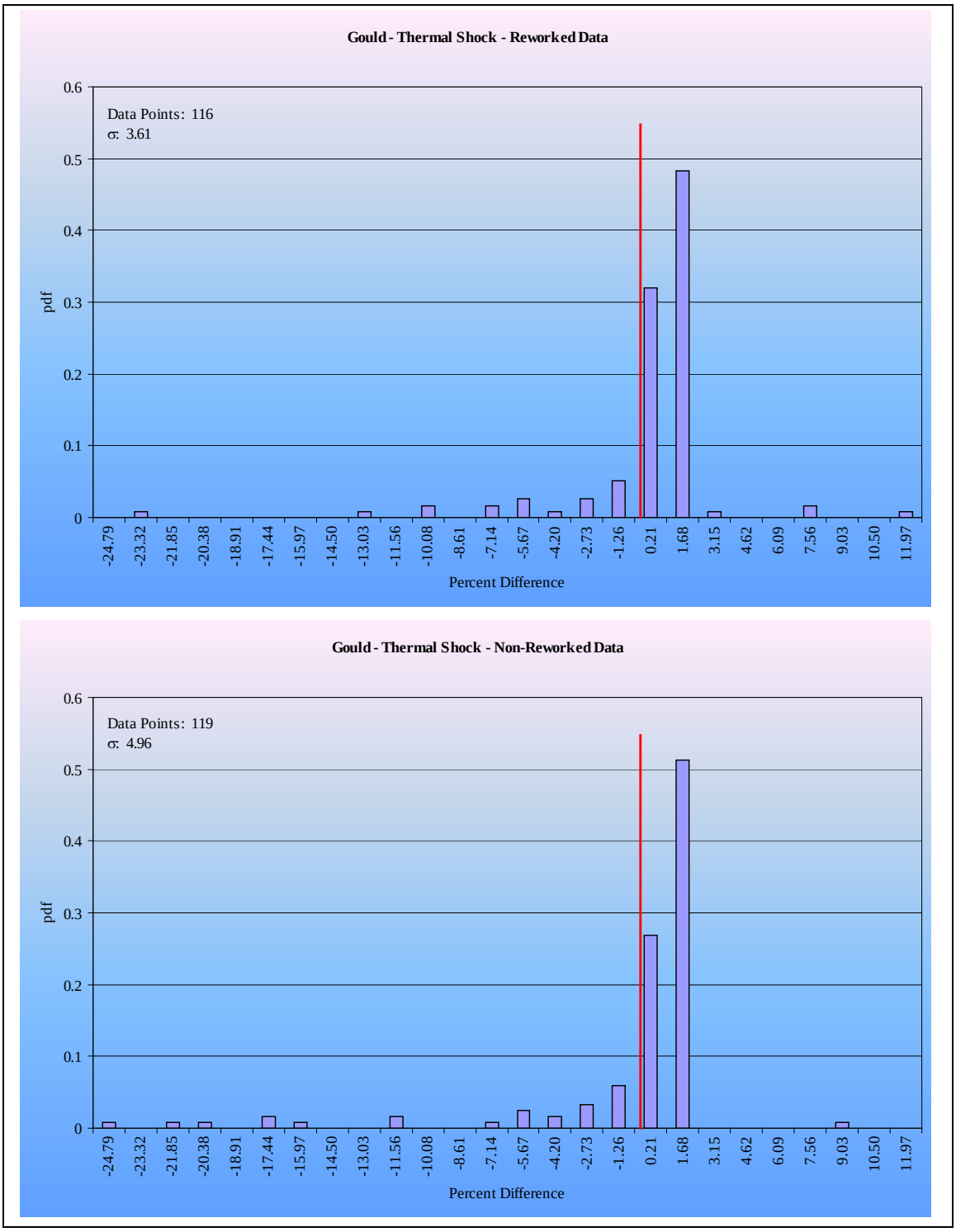


Figure B.15: Gould embedded resistor thermal shock analysis after 500 cycles sorted by rework

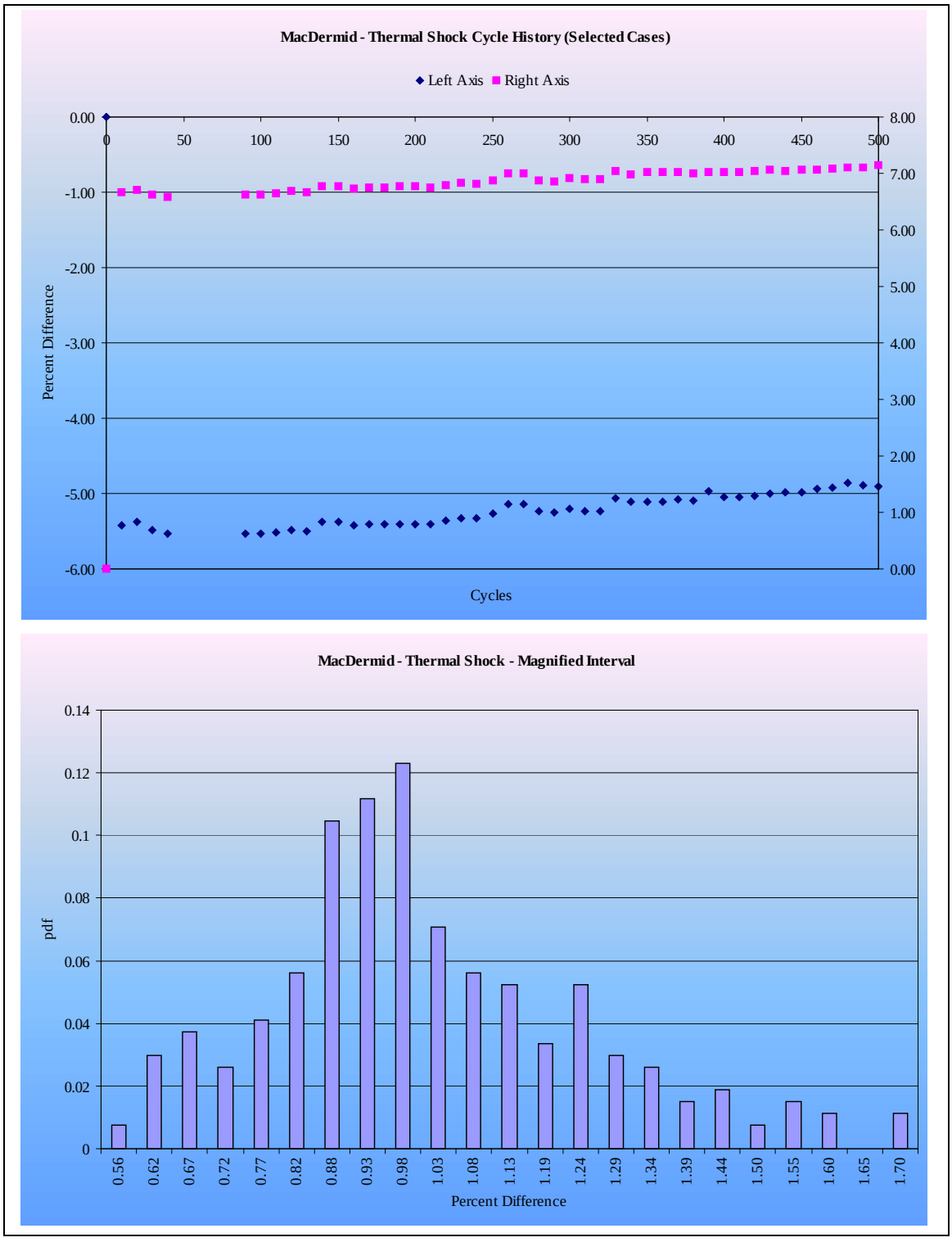


Figure B.16: MacDermid embedded resistor thermal shock analysis after 500 cycles

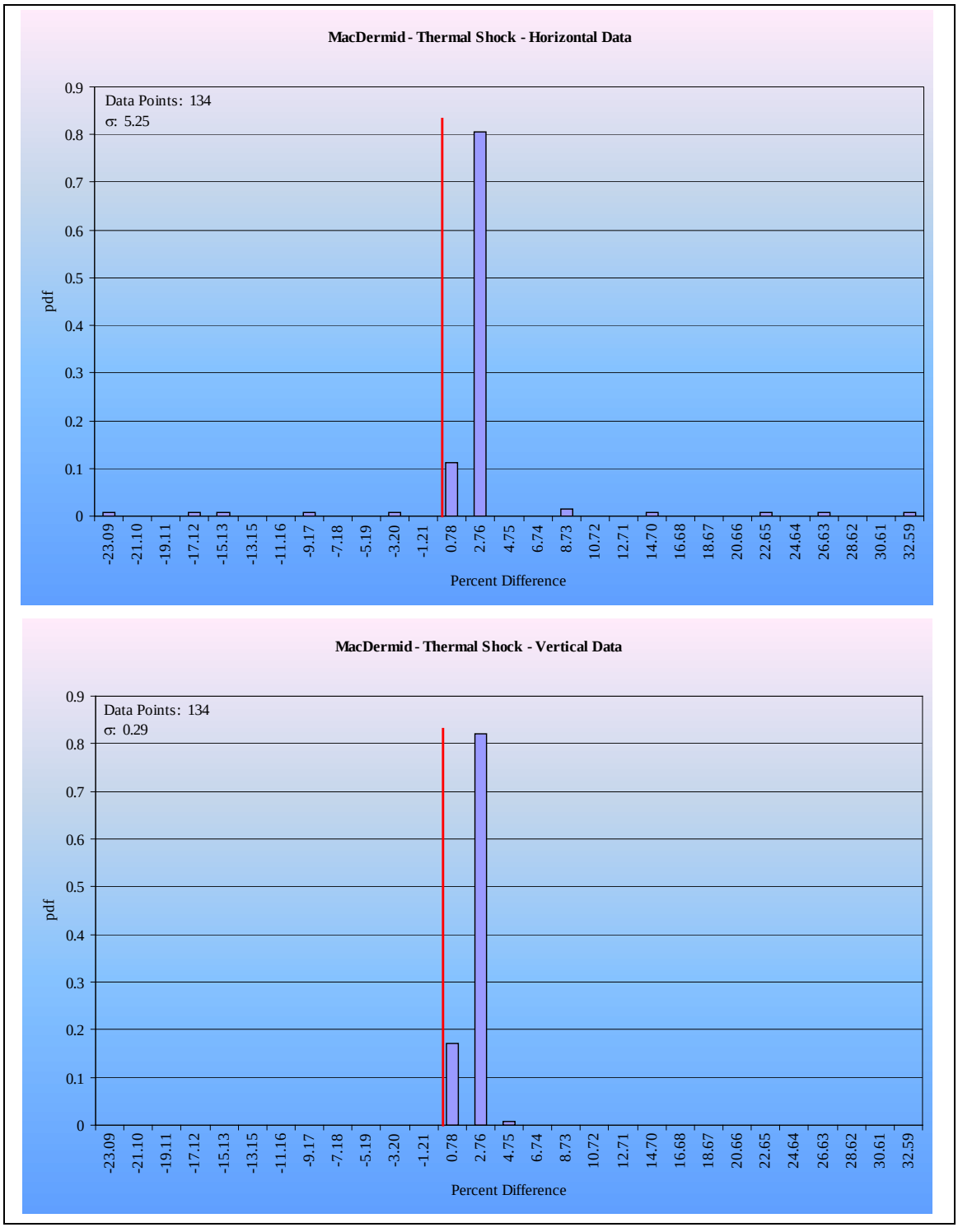


Figure B.17: MacDermid embedded resistor thermal shock analysis after 500 cycles sorted by orientation

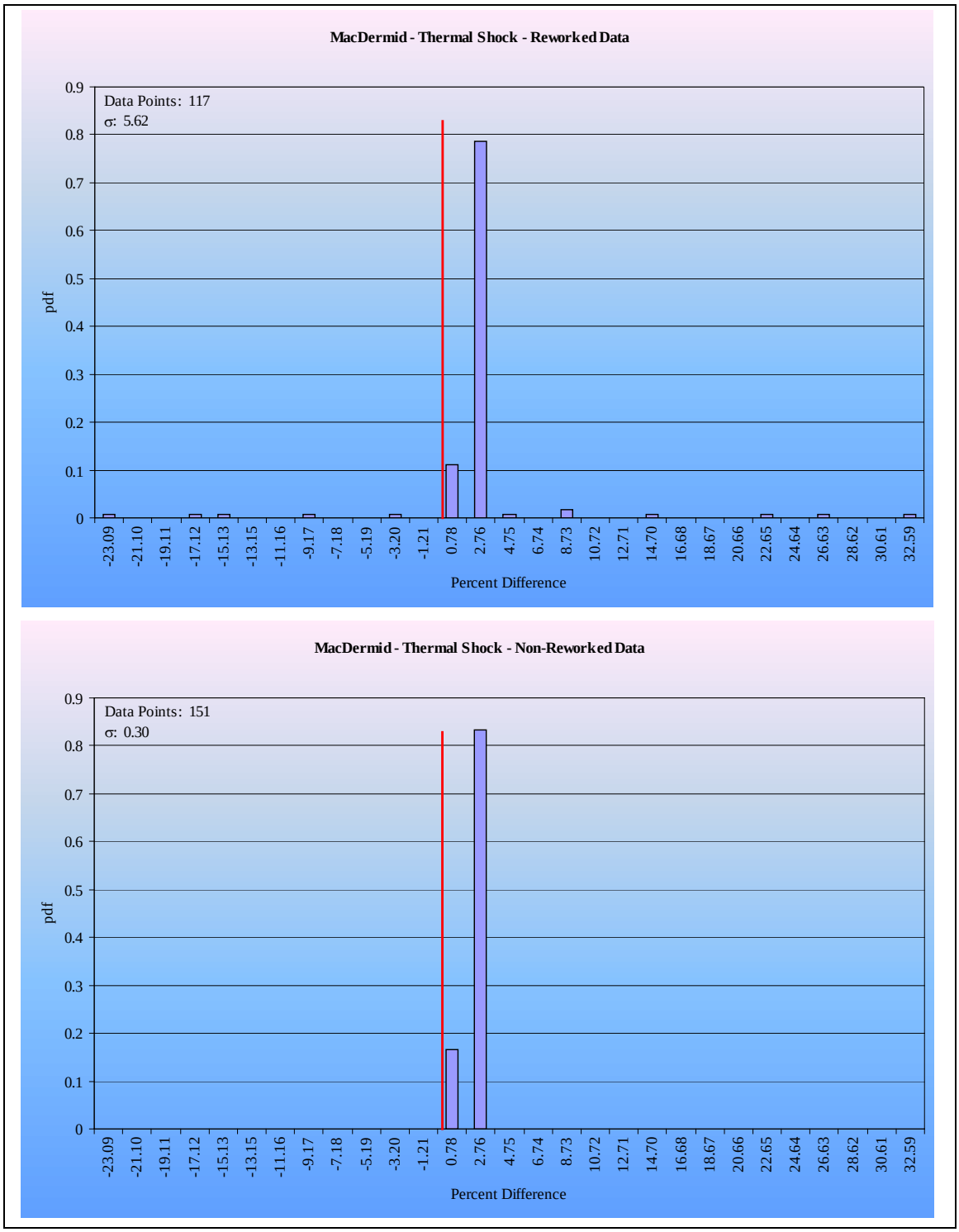


Figure B.18: MacDermid embedded resistor thermal shock analysis after 500 cycles sorted by rework

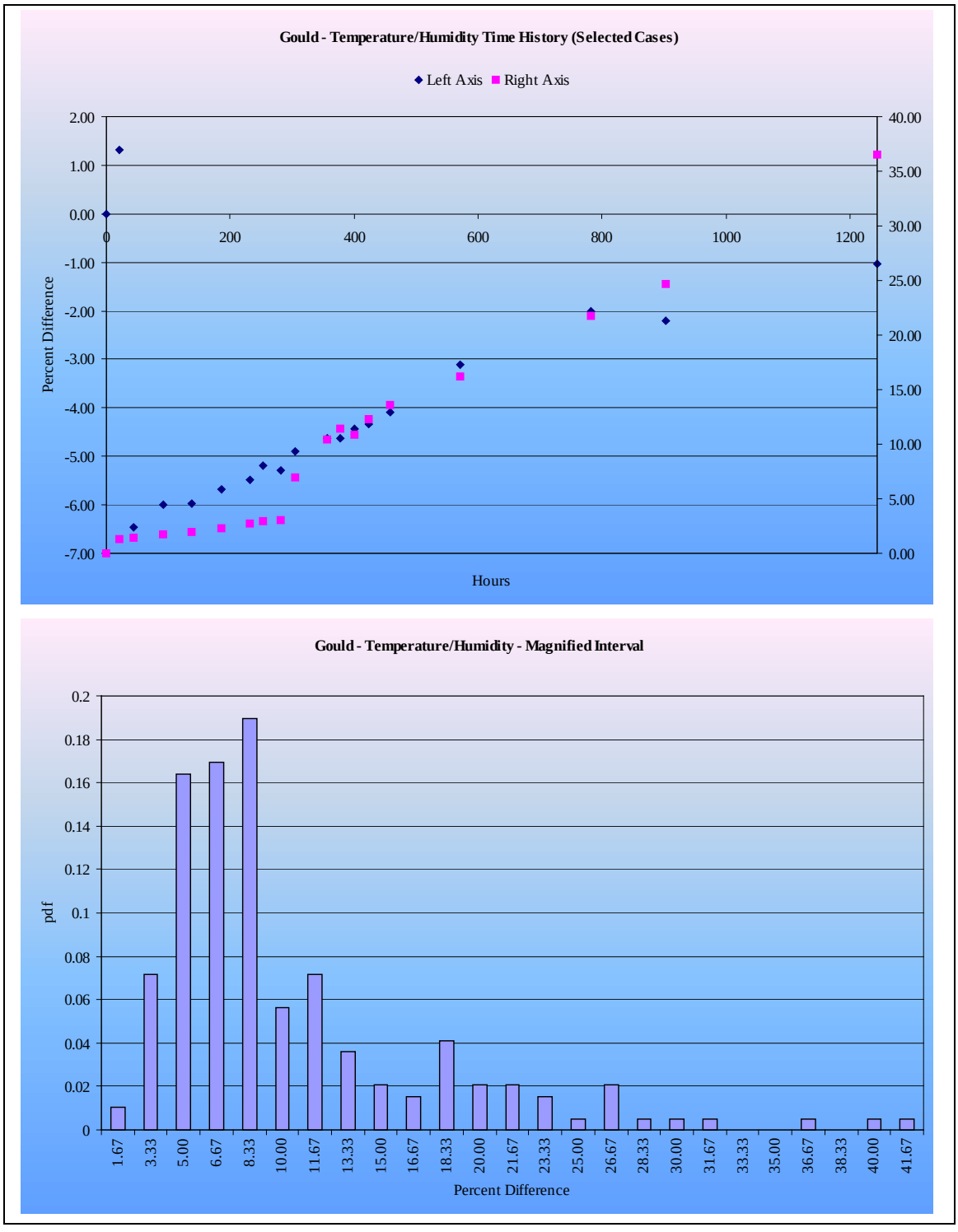


Figure B.19: Gould embedded resistor temperature/humidity analysis after 1244 hours

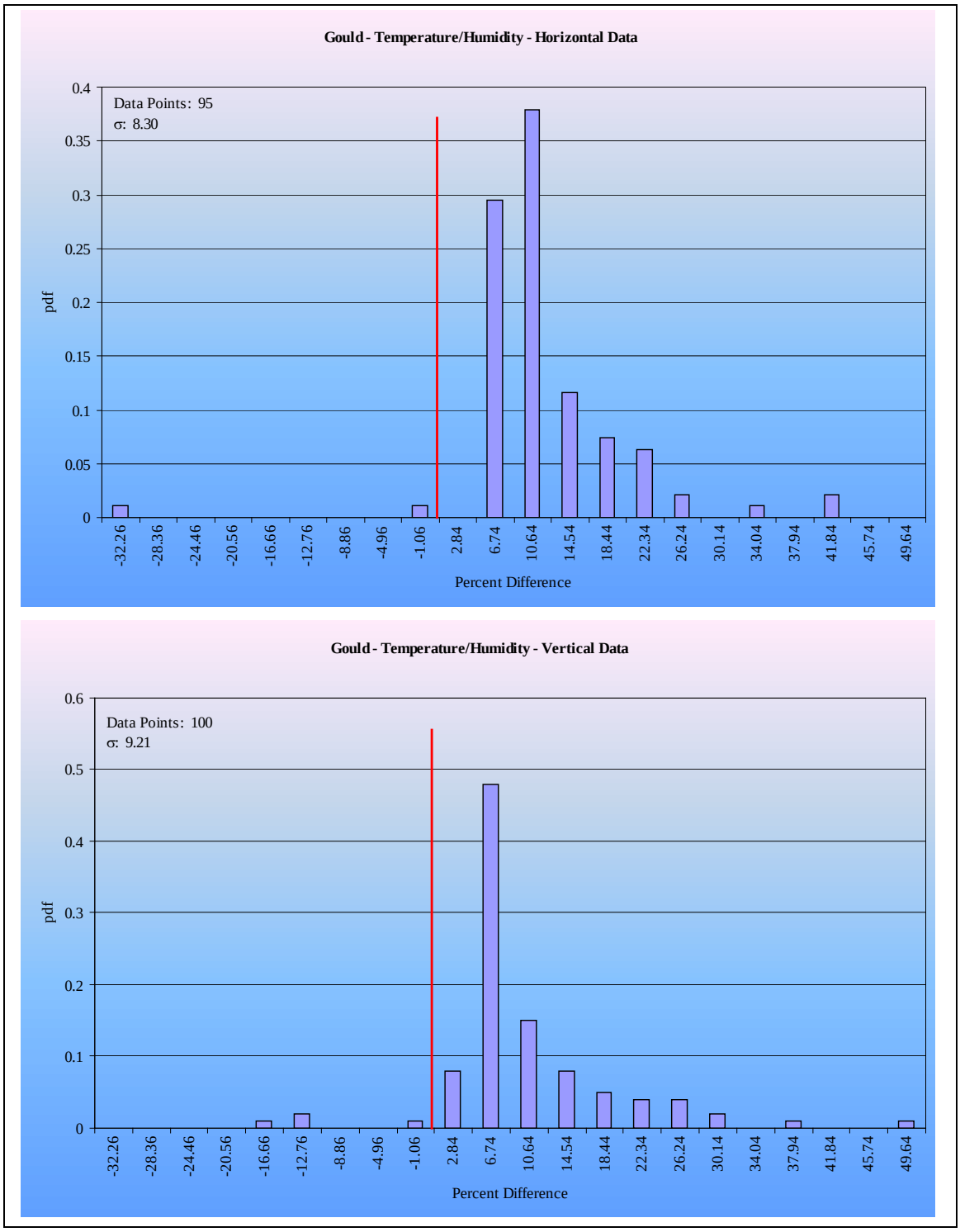


Figure B.20: Gould embedded resistor temperature/humidity analysis after 1244 hours sorted by orientation

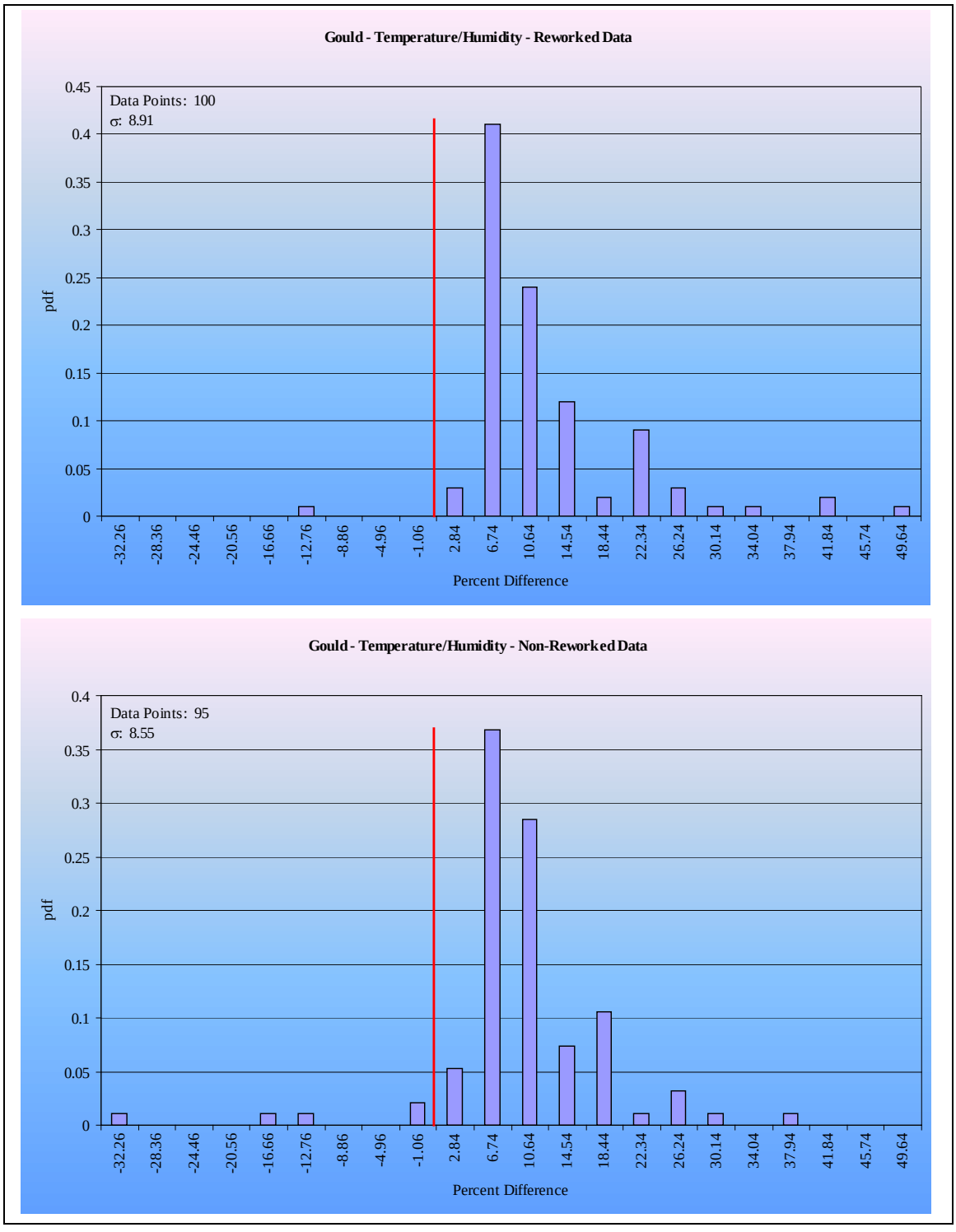


Figure B.21: Gould embedded resistor temperature/humidity analysis after 1244 hours sorted by rework

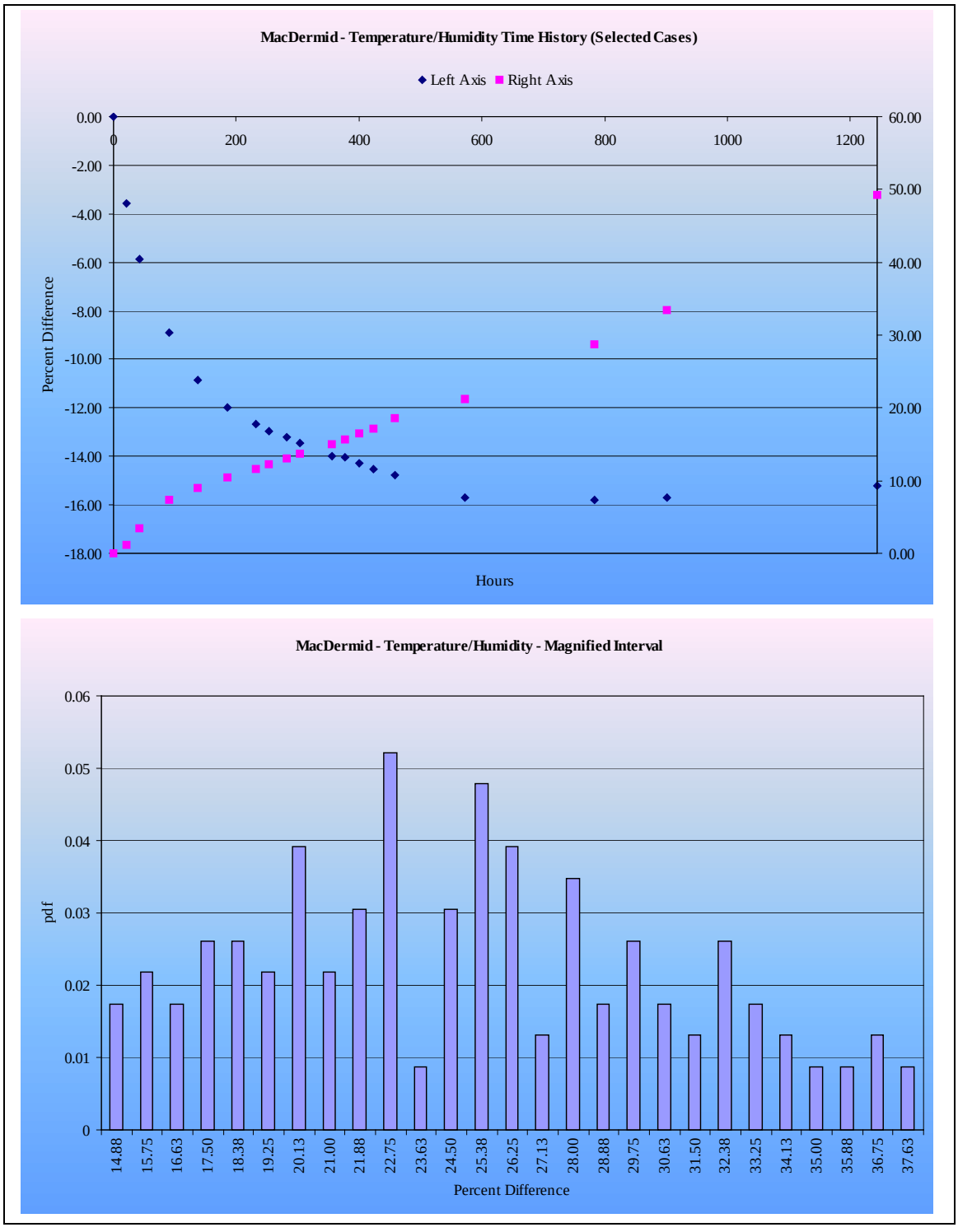


Figure B.22: MacDermid embedded resistor temperature/humidity analysis after 1244 hours

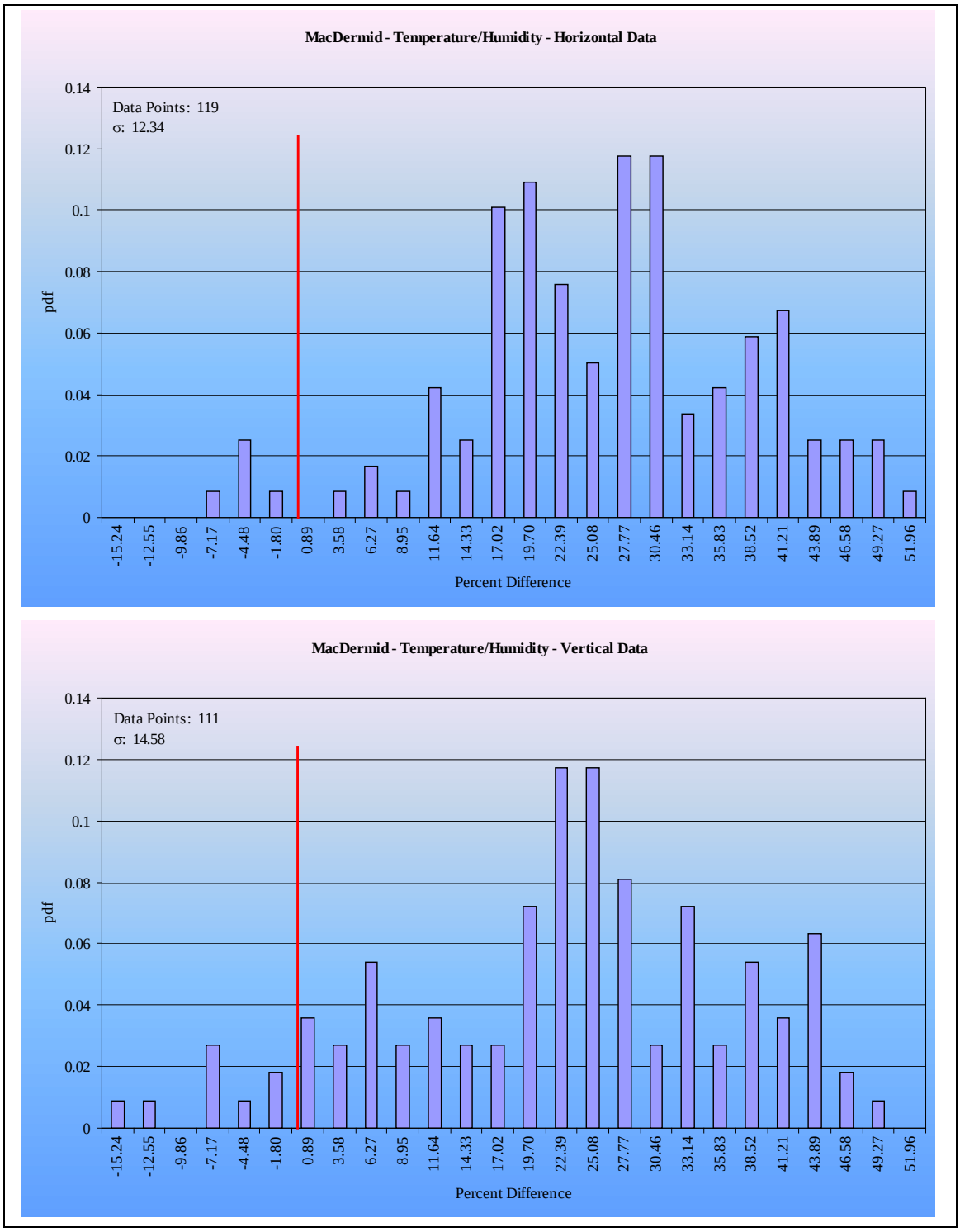


Figure B.23: MacDermid embedded resistor temperature/humidity analysis after 1244 hours sorted by orientation

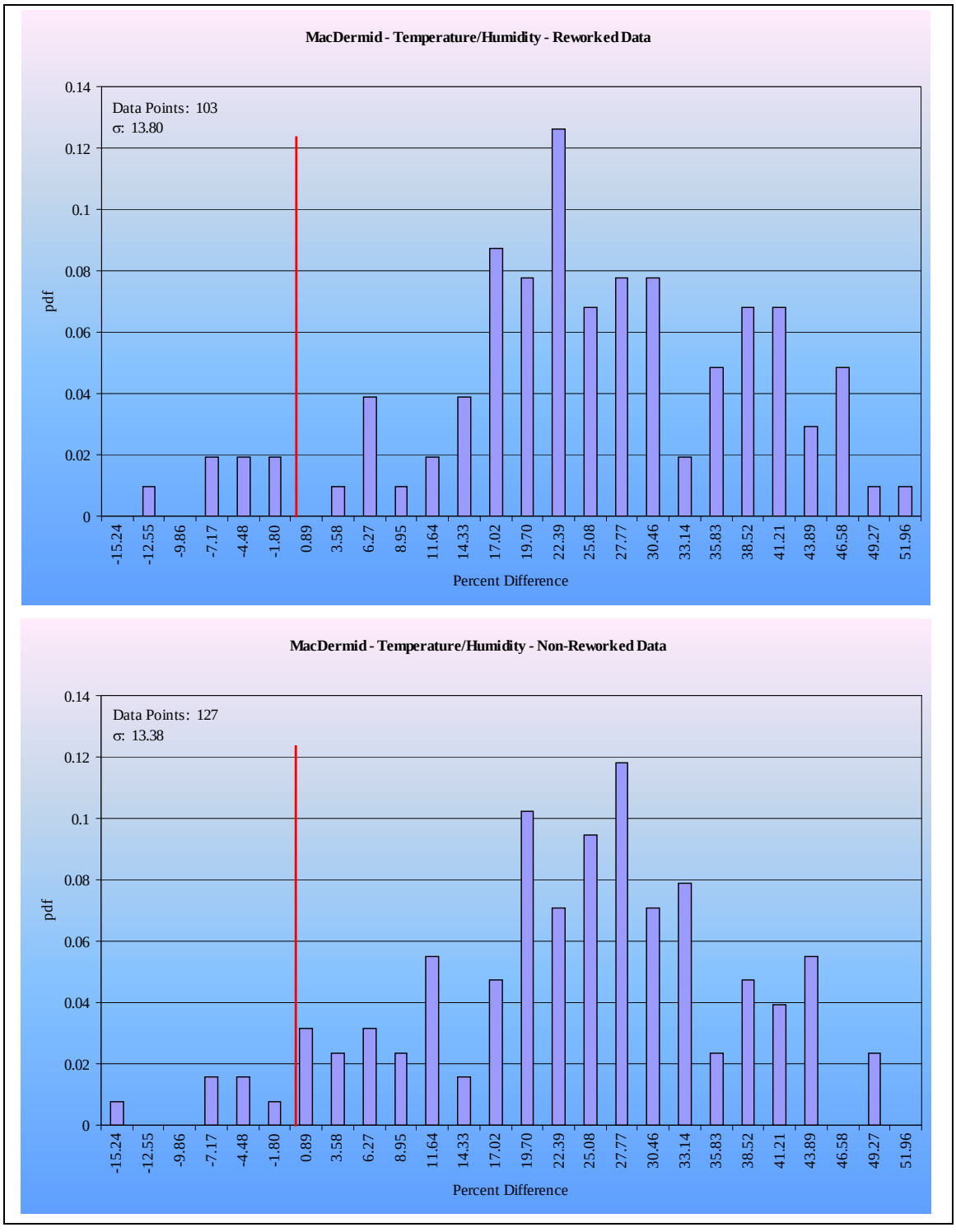


Figure B.24: MacDermid embedded resistor temperature/humidity analysis after 1244 hours sorted by rework

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